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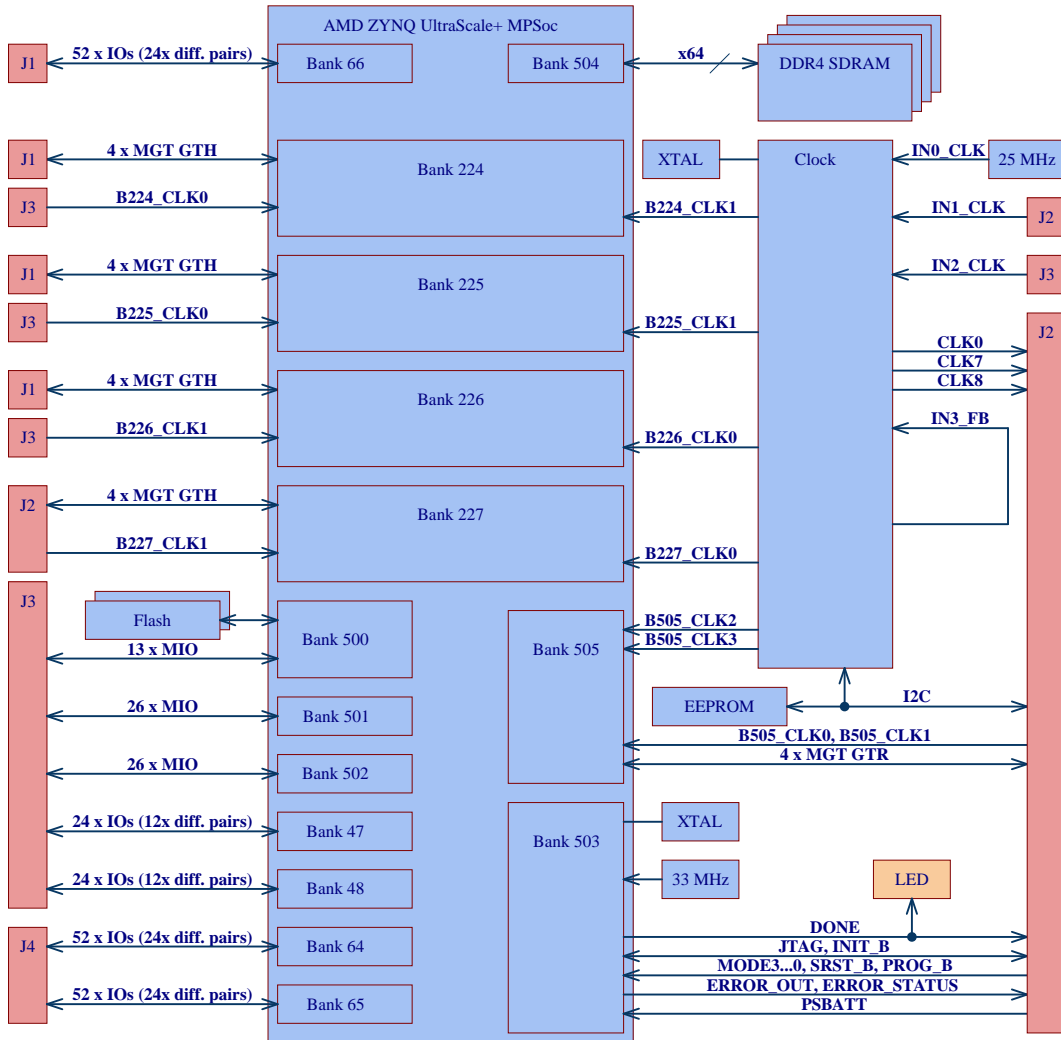
Schematics and other handouts serve for informational purposes only!

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| REV | DATE | Description | VT |
|-----|---------|--|----|
| -01 | 2021-05 | Initial revision | VT |
| | 2022-05 | Changed DCDC U4 TPS548A28 to MPQ8633BGLE-Z Changed C132 100nF to 1nF | |
| | 2022-11 | Added Table with Supported Voltage Ranges | |
| -02 | 2024-04 | <p>1) Changed DCDC (U13) from EN6347QI to MPM3860GQW-Z and updated according circuit..</p> <p>2) Connected DDR4-TEN signals together for (U2A), (U3A), (U9A), and (U12A) and pulled them low via 499 Ohm resistor (R127). Added testpoint (TP3) for signal (DDR4-TEN).</p> <p>3) Changed voltage rail from 1.35 V to 1.45 V via adaption voltage divider resistor (R30) and changed voltage rail name PL_GT_1V35 to (PL_GT_1V45).</p> <p>4) Changed voltage rail from 1.05 V to 1.15 V via adaption voltage divider resistors (R33) and (R35) and changed voltage rail name PL_GT_1V05 to (PL_GT_1V15).</p> <p>5) Added diode (D2) between (U41) pin 3 net (MR) and voltage rail (3.3VIN).</p> <p>6) Added capacitors (C202) ... (C205) for VTT voltage rail (VTT).</p> <p>7) Added resistors (R124) (default: not fitted) and (R125) to supply (U4) VCC either from (PL_DCIN) or from (3.3VIN).</p> <p>8) Changed resistor (R76) from 4.22 kOhm to 9.09 kOhm to set current limit to nearly 14.3 A for (U4).</p> <p>9) Changed inductor (L9) from XGL4030-301MEC to XGL5030-351MEC.</p> <p>10) Added remote sense option (default: not fitted):</p> <p>10.1) (R126) for (U30).</p> <p>10.2) (R128) for (U29).</p> <p>10.3) (R129) for (U31).</p> <p>11) Added decoupling capacitors:</p> <p>11.1) (C208) for (U4).</p> <p>11.2) (C211), (C212), and (C213) for (U6).</p> <p>11.3) (C216) for (U10).</p> <p>11.4) (C214) for (U26).</p> <p>11.5) (C215) for (U27).</p> <p>11.6) (C210) for (U34).</p> <p>11.7) (C196) for (U39).</p> <p>11.8) (C197) for (U40).</p> <p>11.9) (C198) for (U42).</p> <p>11.10) (C199) for (U41).</p> <p>11.11) (C200) for (U44).</p> <p>11.12) (C201), (C206), and (C207) for (U1N).</p> <p>12) Added pull-up resistors for HOLD ((R130)) and WP ((R131)) signals for Flash (U7A).</p> <p>13) Added pull-up resistors for HOLD ((R132)) and WP ((R133)) signals for Flash (U17A).</p> <p>14) Changed capacitor ((C132)) from 1 nF, X7R to 1.2 nF, NP0.</p> <p>15) Changed 10 nF capacitor ((C112)) from 16 V, 0402 to 10 V, 0201.</p> <p>16) Changed 100 nF capacitors ((C37), (C95), (C96), (C130), and (C131)) from 6.3 V, X5R, 0201 to 50 V, X7R, 0402.</p> <p>17) Changed capacitor ((C76), (C77), (C134), (C195)) from 1 µF, 16 V to 2.2 µF, 10 V.</p> <p>18) Changed capacitor ((C129), (C140), (C141), (C142), (C143), (C144), (C145), (C146), (C147), (C148), (C153)) from 10 µF, 16 V to 22 µF, 10 V.</p> <p>19) Changed 22 µF capacitor ((C70), (C73), (C74), (C75)) from 0805 to 0603.</p> <p>20) Changed 22 µF capacitor ((C78), (C80), (C81), (C82), (C83), (C84), (C85), (C86), (C87), (C110), (C152), (C154), (C178)) from 6.3 V to 10 V.</p> <p>21) Changed 100 Ohm resistors ((R7), (R10)) from 0201, 0.05 W to 0402, 0.063 W.</p> <p>22) Changed resistor (R77) from 12 kOhm to 10 kOhm.</p> <p>23) Changed resistors (R41) and (R58) from 2 kOhm to 2.49 kOhm.</p> <p>24) Added testpoints (TP4), (TP10), (TP11), (TP13), (TP14), (TP19), (TP21), (TP22), (TP33) ... (TP72).</p> <p>25) Added UKCA logo.</p> <p>26) Updated from library.</p> <p>27) Changed signal trace length.</p> <p>28) Updated documentation.</p> | ED |



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Supported Voltage Ranges:

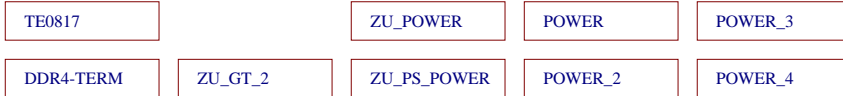
| Power Rail | Direction | Range | Tolerance | Description | Note |
|------------|-----------|---------------|-----------|-------------------|---------------------------|
| 3.3VIN | IN | 3.3 V | +/- 5 % | Micromodule Power | - |
| PL_DCIN | IN | 3.3 V - 5.0 V | +/- 5 % | Micromodule Power | Programmable Logic |
| LP_DCDC | IN | 3.3 V - 5.0 V | +/- 3 % | Micromodule Power | Low-Power Domain |
| GT_DCDC | IN | 3.3 V - 5.0 V | +/- 3 % | Micromodule Power | GTH/GTY Transceiver |
| DCDCIN | IN | 3.3 V - 5.0 V | +/- 5 % | Micromodule Power | Full-Power Domain and GTR |
| VCCO_64 | IN | 1.0 V - 1.8 V | +/- 3 % | HP IO Bank 64 | - |
| VCCO_65 | IN | 1.0 V - 1.8 V | +/- 3 % | HP IO Bank 65 | - |
| VCCO_66 | IN | 1.0 V - 1.8 V | +/- 3 % | HP IO Bank 66 | - |
| VCCO_47 | IN | 1.2 V - 3.3 V | +/- 3 % | HD IO Bank 47 | - |
| VCCO_48 | IN | 1.2 V - 3.3 V | +/- 3 % | HD IO Bank 48 | - |
| PSBATT | IN | 1.2 V - 1.5 V | - | RTC / BBRAM | - |
| PLL_3V3 | IN | 3.3 V | +/- 5 % | PLL Core Power | - |
| PL_1V8 | OUT | 1.8 V | +/- 3 % | Power for Carrier | Programmable Logic |
| PS_1V8 | OUT | 1.8 V | +/- 3 % | Power for Carrier | Processing System |
| DDR4_1V2 | OUT | 1.2 V | +/- 3 % | Power for Carrier | PS DDR I/O Supply |

I2C Address:

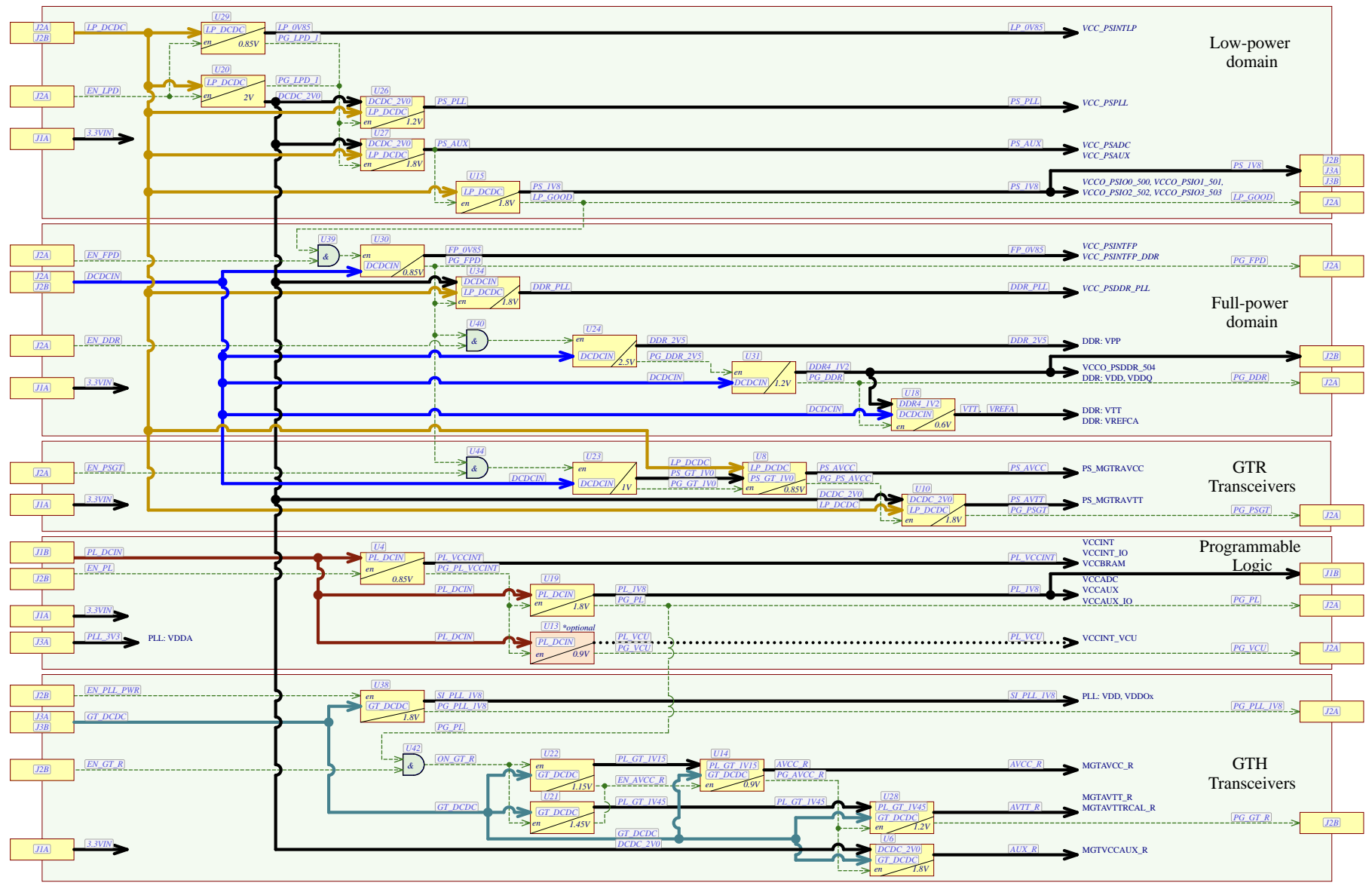
| Device | I2C ADDR | Note |
|-------------------|----------|------|
| PLL U5 | 0x69 | - |
| EEPROM U11 | 0x50 | - |

Legend:

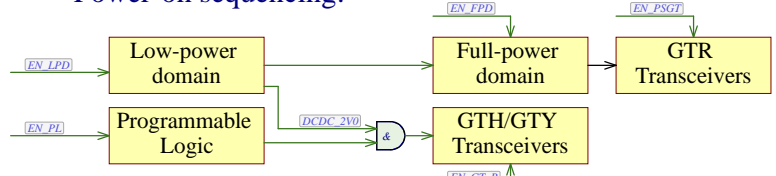
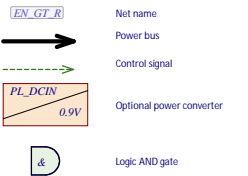
- B2B Connector
- LED Interface
- On-board Components



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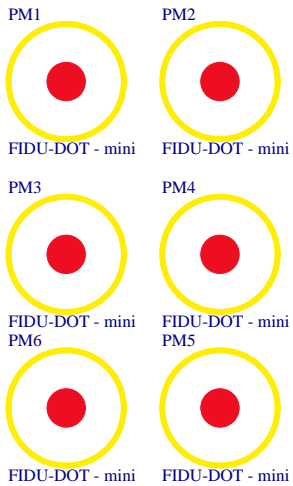


Power-on sequencing:



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Special notes:



Serial1
Serial
Serialnumber 6,3 x 6.3mm
LOGO1

TE Logo PRINT Layer

LOGO PRINT
MECH1

TE Address Overlay

LOGO ADDRESS
CE

CE Logo on Top Overlay

CE-TOPOVERLAY
UKCA

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

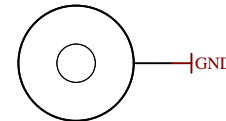
RoHS

RoHS Logo on Top Overlay

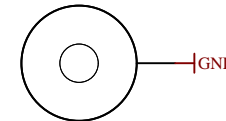
RoHS-TOPOVERLAY
WEEE

WEEE Logo on Top Overlay

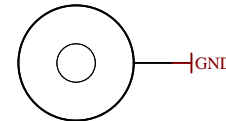
WEEE-TOPOVERLAY



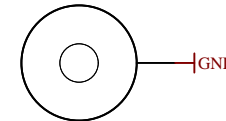
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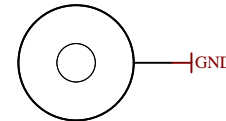
Mount.Hole 3.2mm für Unterlegscheibe



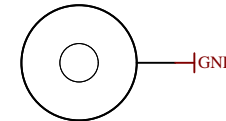
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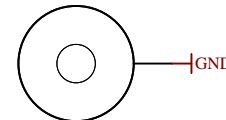
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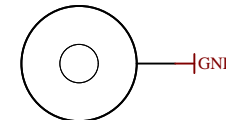
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



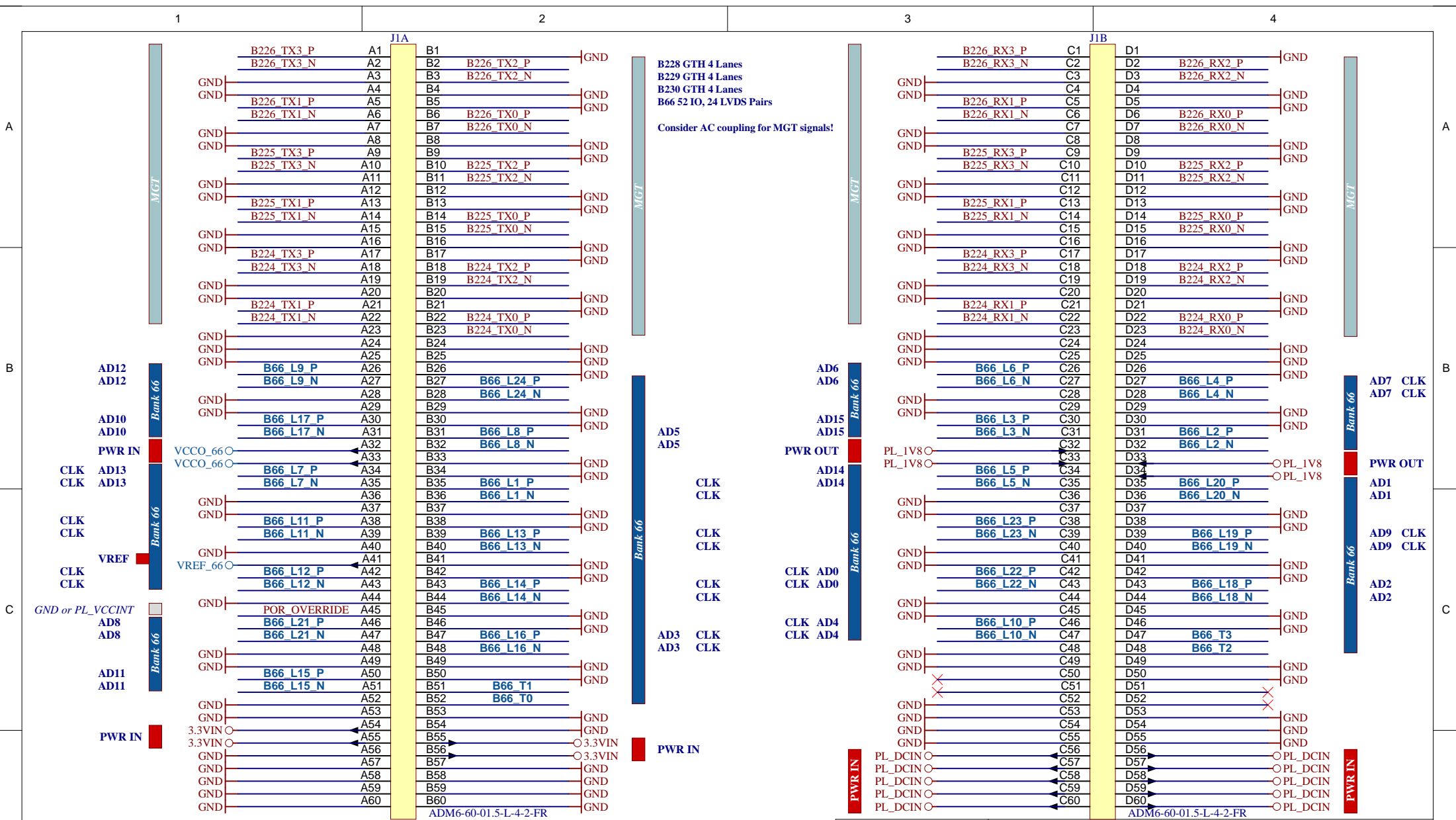
Mount.Hole 3.2mm für Unterlegscheibe

Design drawn by: ED
Checked by: MT

Assembly variant: [No Variations]
Created by:
Modified by:
Modified at:



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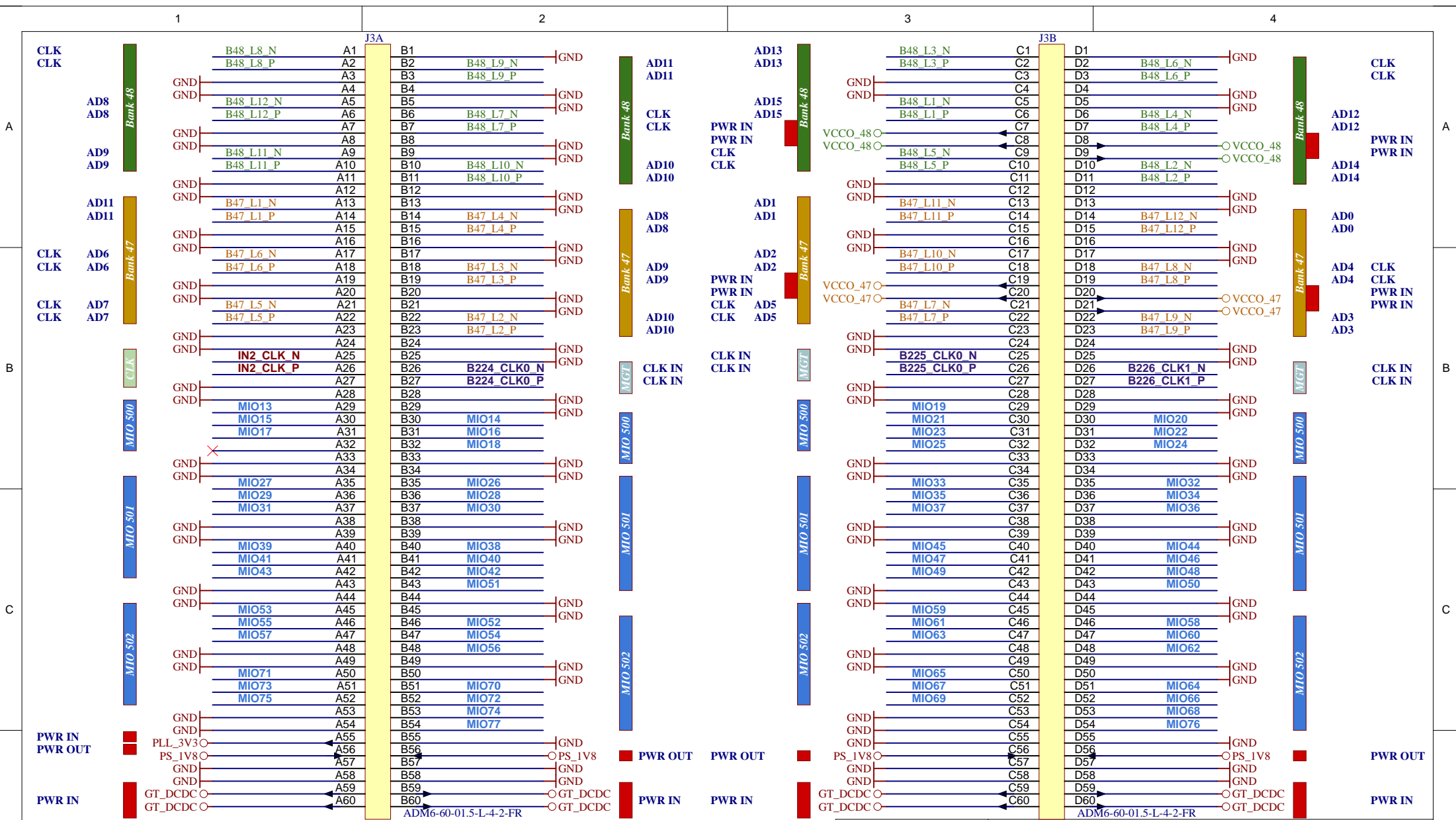


- Bank 47 HD 0..VCC047
- Bank 48 HD 0..VCC048
- Bank 64 HP 0..VCC064
- Bank 65 HP 0..VCC065
- Bank 66 HP 0..VCC066

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Filename: **J1.SchDoc**



- Bank 47 HD 0..VCC047 B47 24 IO, 12 LVDS Pairs
 - Bank 48 HD 0..VCC048 B48 24 IO, 12 LVDS Pairs
 - Bank 64 HP 0..VCC064 B228 GTH CLK IN
 - Bank 65 HP 0..VCC065 B229 GTH CLK IN
 - Bank 66 HP 0..VCC066 B230 GTH CLK IN
- 65 MIO
PLL CLK IN



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1

2

3

4

1

2

3

4

A

B

C

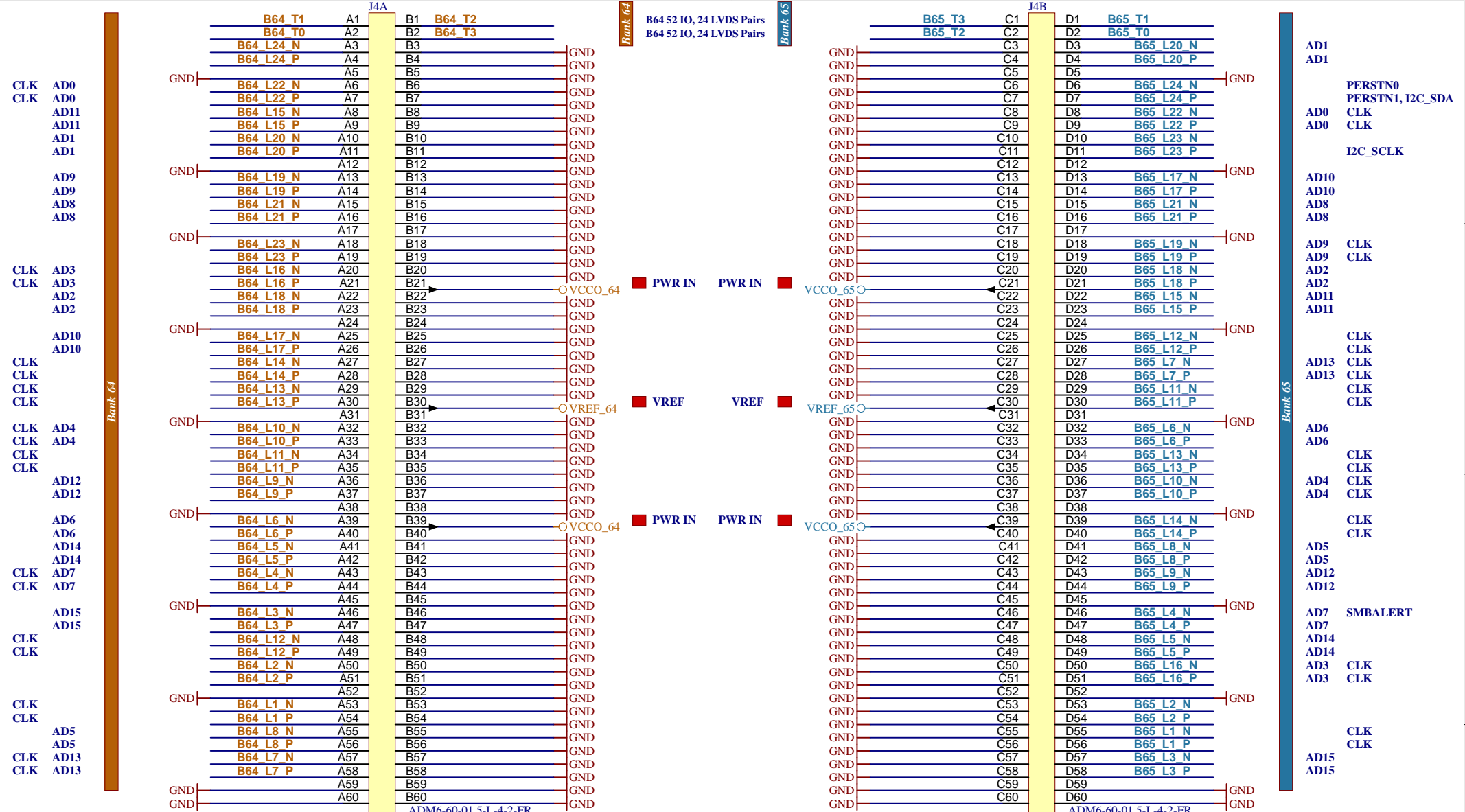
D

A

B

C

D



- Bank 47 HD 0..VCCO47
- Bank 48 HD 0..VCCO48
- Bank 64 HP 0..VCCO64
- Bank 65 HP 0..VCCO65
- Bank 66 HP 0..VCCO66



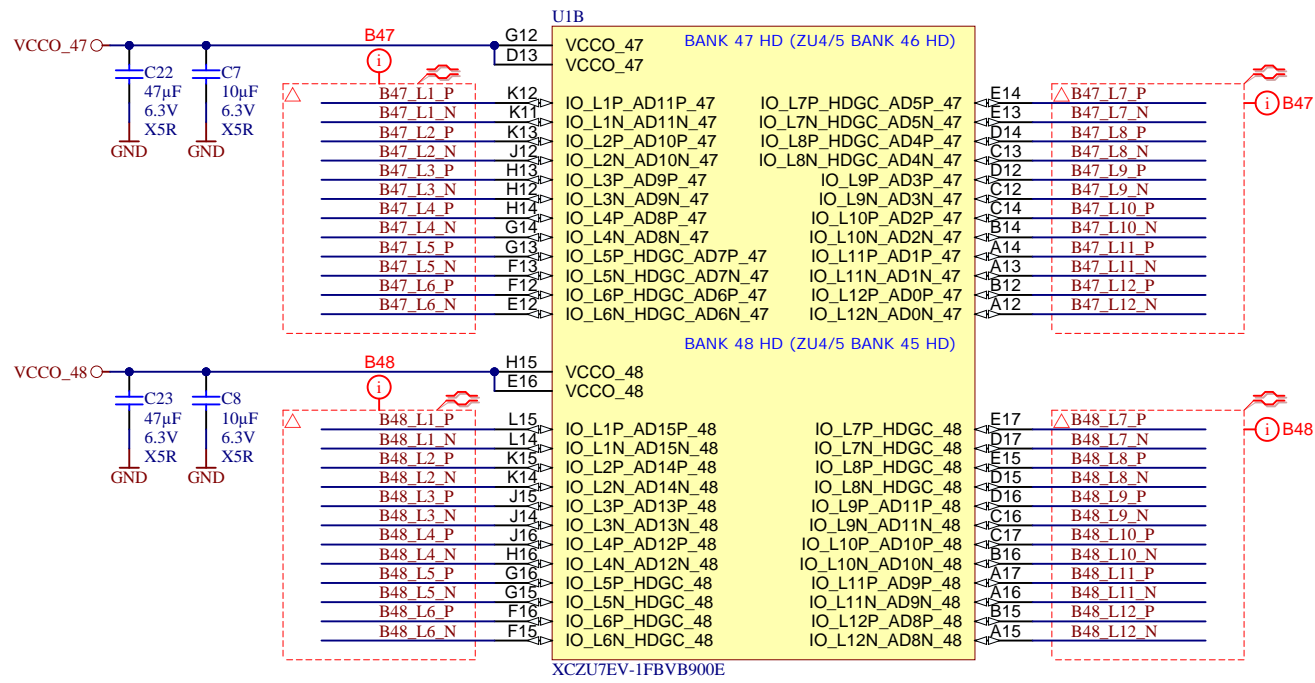
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1

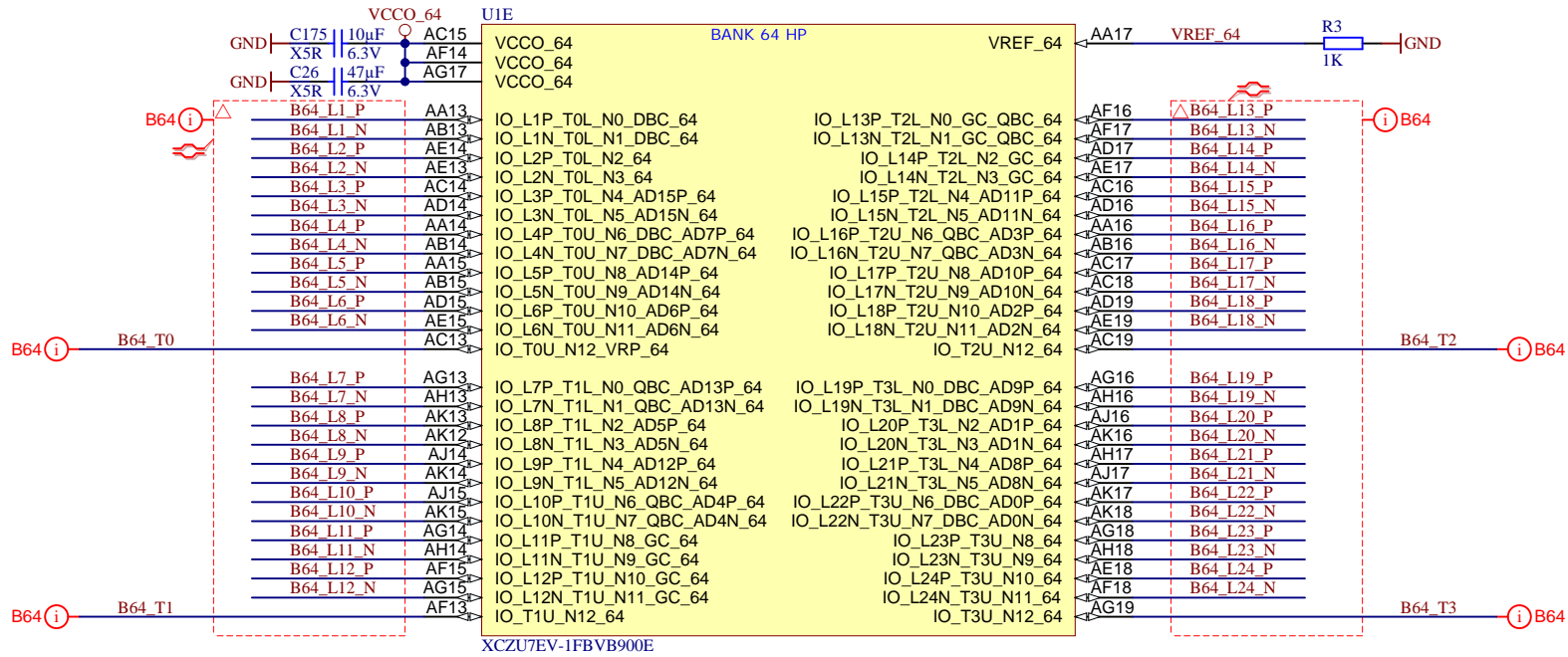
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3

4



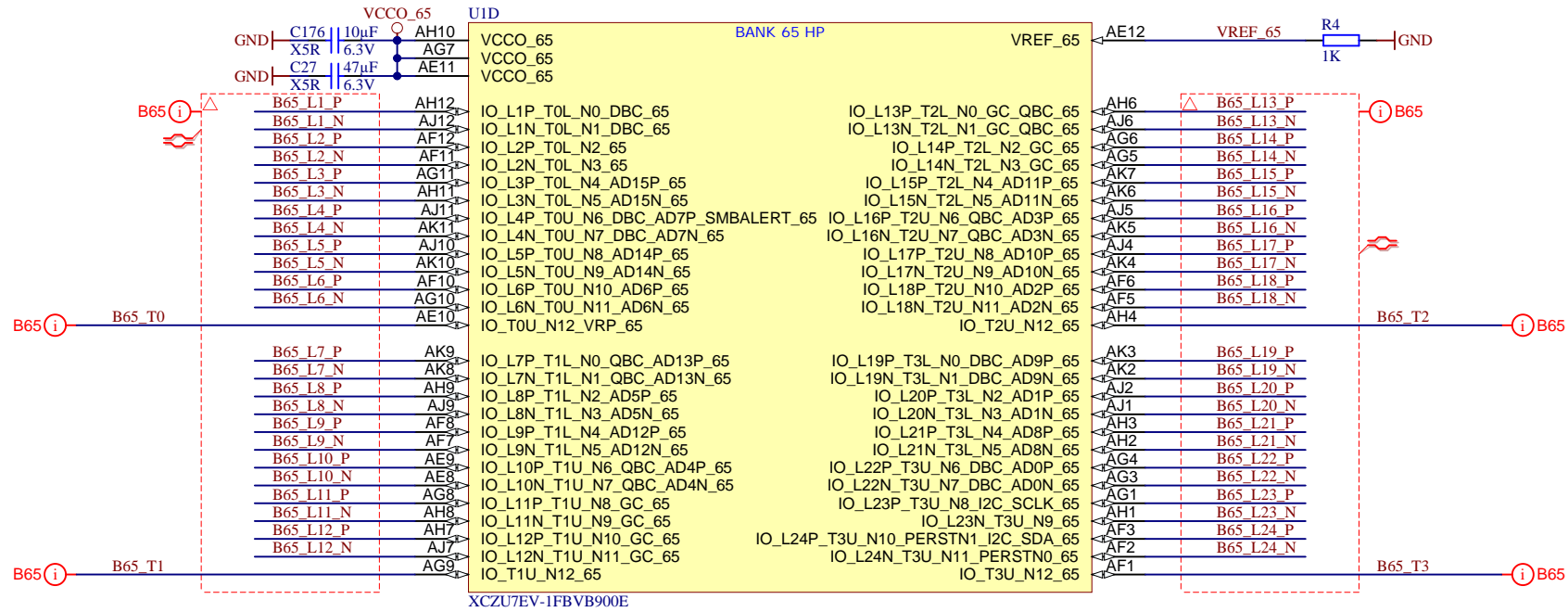
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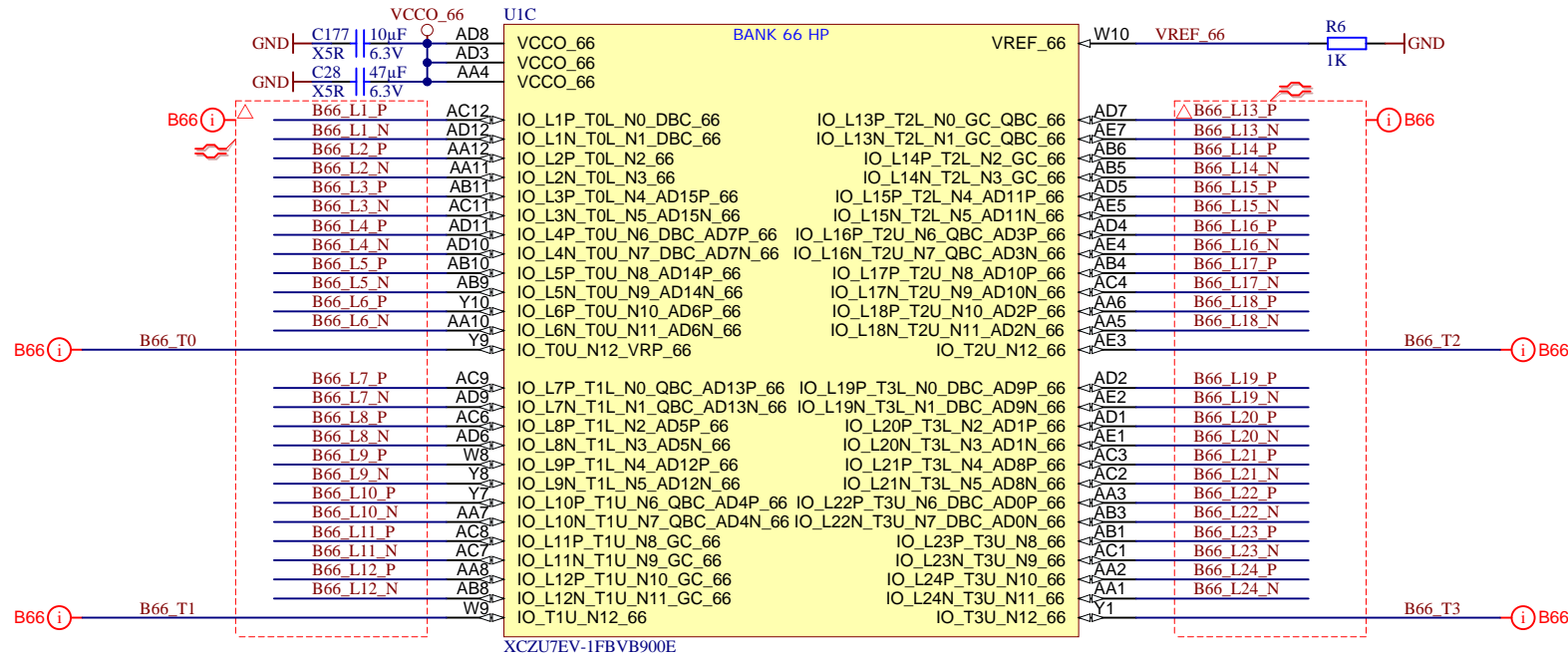
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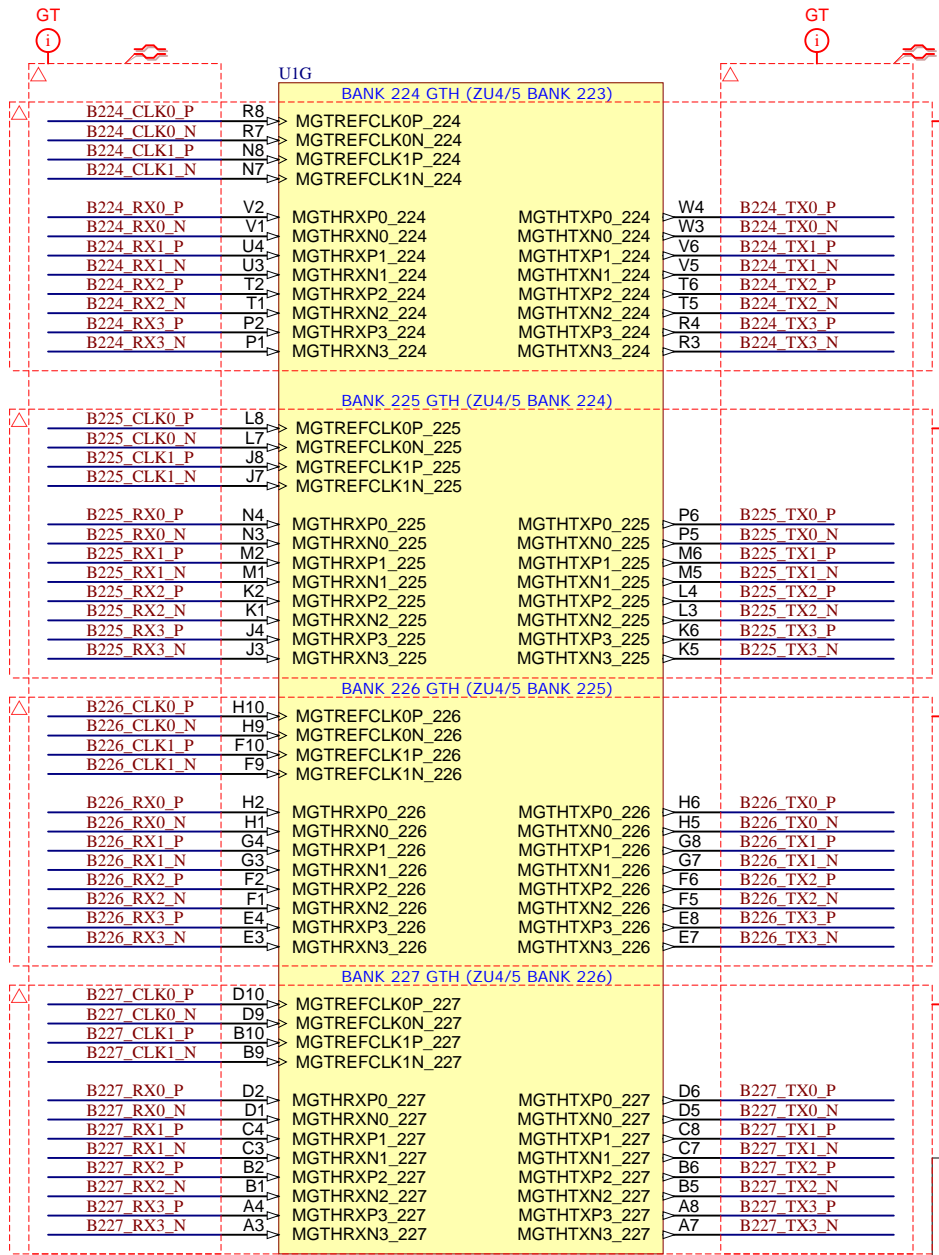
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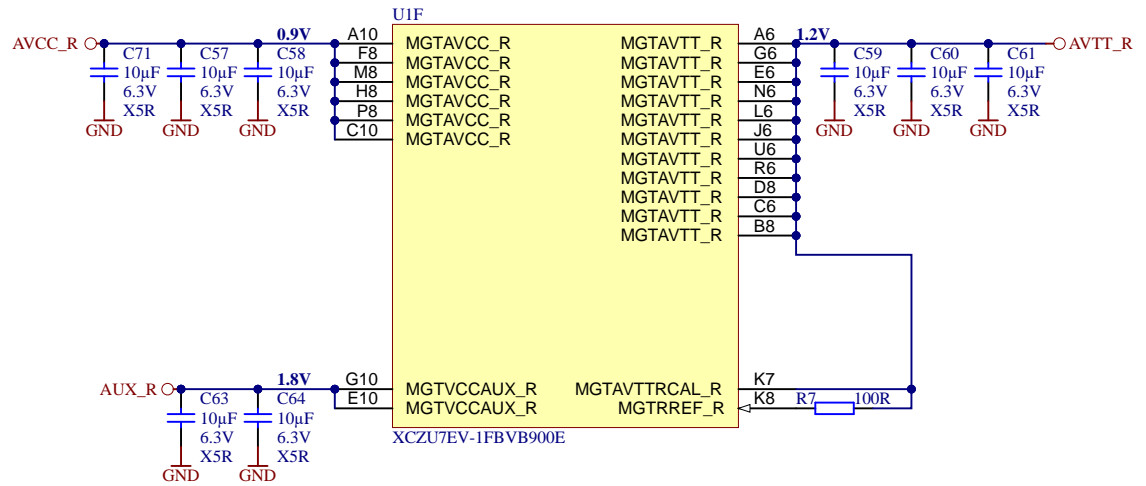
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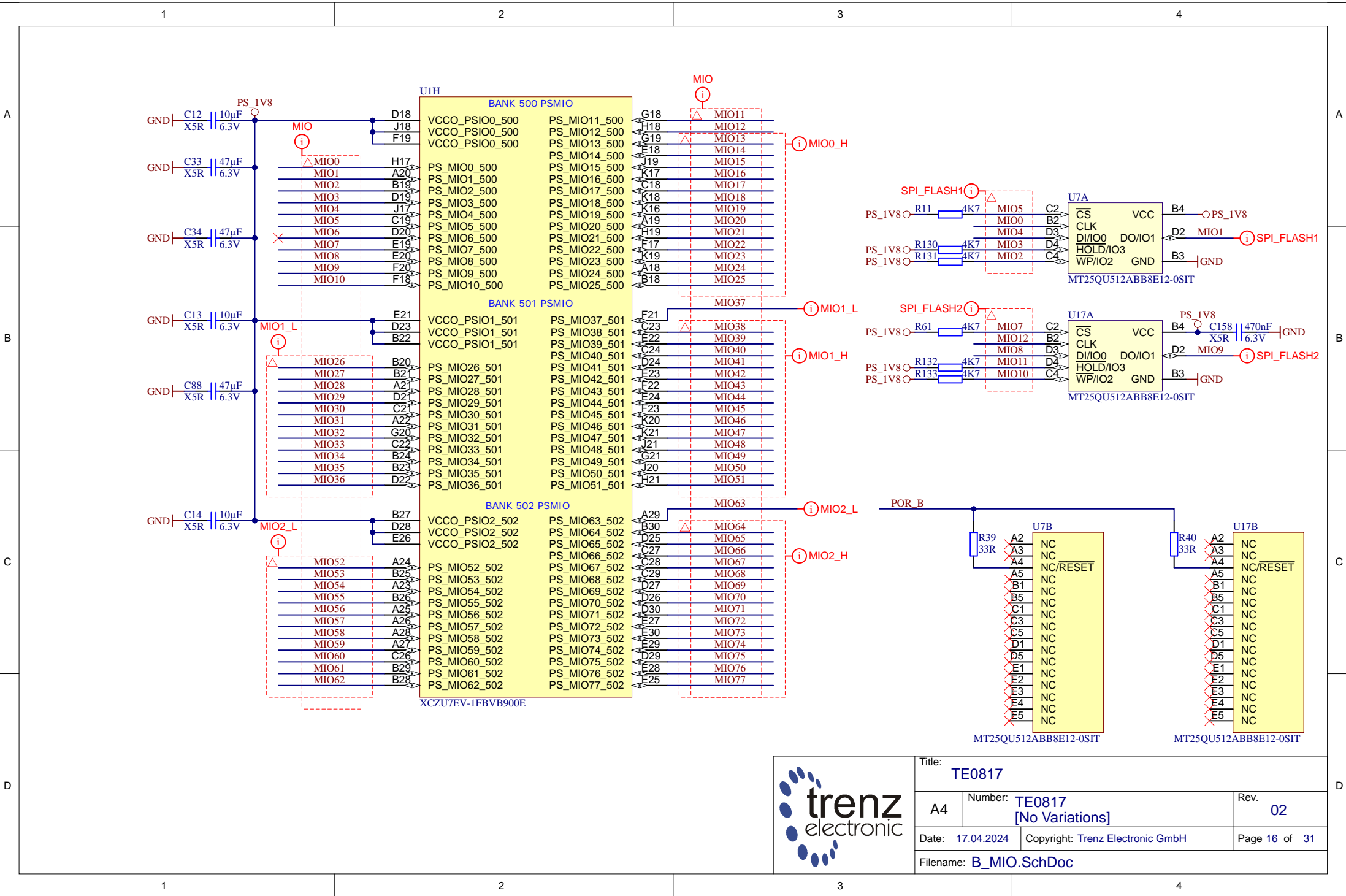
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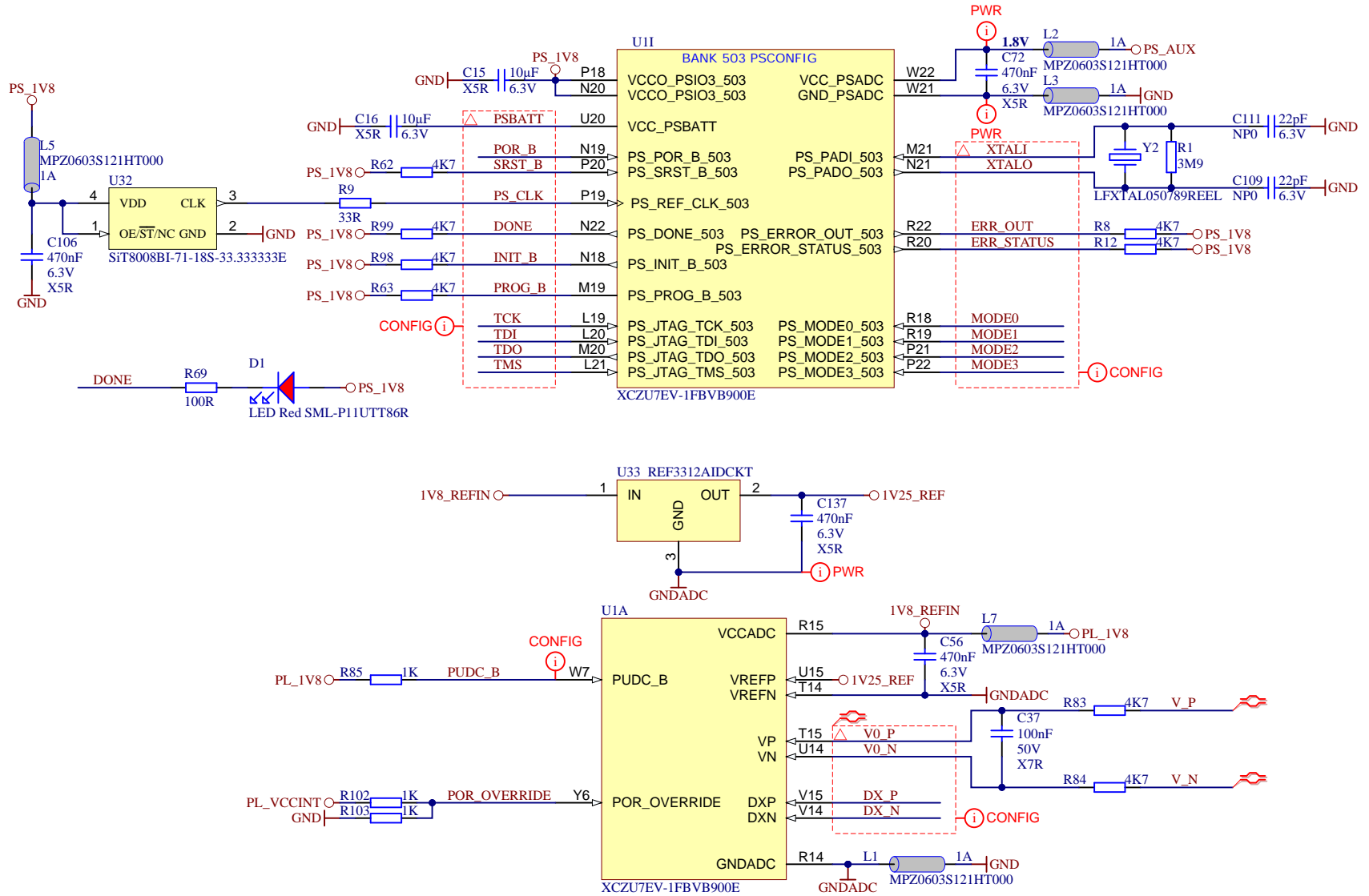
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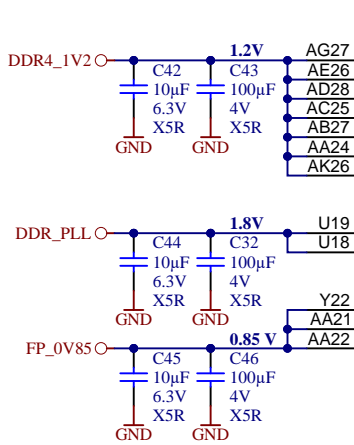
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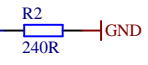
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UIJ BANK 504 PSDDR

| | | | |
|----------------------|------------------|------|-------------|
| VCCO_PSDDR_504 | PS_DDR_CK0_504 | AE30 | DDR4-CLK0_P |
| VCCO_PSDDR_504 | PS_DDR_CK_N0_504 | AF30 | DDR4-CLK0_N |
| VCCO_PSDDR_504 | PS_DDR_CKE0_504 | AC30 | DDR4-CKE0 |
| VCCO_PSDDR_504 | | AF28 | |
| VCCO_PSDDR_504 | PS_DDR_CK1_504 | AG28 | |
| VCCO_PSDDR_504 | PS_DDR_CK_N1_504 | AB28 | |
| VCCO_PSDDR_504 | PS_DDR_CKE1_504 | | |
| VCC_PSDDR_PLL | PS_DDR_A0_504 | AH30 | DDR4-A0 |
| VCC_PSDDR_PLL | PS_DDR_A1_504 | AG30 | DDR4-A1 |
| VCC_PSDDR_PLL | PS_DDR_A2_504 | AK29 | DDR4-A2 |
| VCC_PSINTFP_DDR | PS_DDR_A3_504 | AJ30 | DDR4-A3 |
| VCC_PSINTFP_DDR | PS_DDR_A4_504 | AK28 | DDR4-A4 |
| VCC_PSINTFP_DDR | PS_DDR_A5_504 | AK27 | DDR4-A5 |
| VCC_PSINTFP_DDR | PS_DDR_A6_504 | AF27 | DDR4-A6 |
| VCC_PSINTFP_DDR | PS_DDR_A7_504 | AE27 | DDR4-A7 |
| VCC_PSINTFP_DDR | PS_DDR_A8_504 | AF26 | DDR4-A8 |
| VCC_PSINTFP_DDR | PS_DDR_A9_504 | AG26 | DDR4-A9 |
| VCC_PSINTFP_DDR | PS_DDR_A10_504 | AE29 | DDR4-A10 |
| VCC_PSINTFP_DDR | PS_DDR_A11_504 | AE28 | DDR4-A11 |
| VCC_PSINTFP_DDR | PS_DDR_A12_504 | AH29 | DDR4-A12 |
| VCC_PSINTFP_DDR | PS_DDR_A13_504 | AG29 | DDR4-A14 |
| VCC_PSINTFP_DDR | PS_DDR_A14_504 | AJ29 | DDR4-A15 |
| VCC_PSINTFP_DDR | PS_DDR_A15_504 | AH27 | DDR4-A16 |
| VCC_PSINTFP_DDR | PS_DDR_A16_504 | AJ27 | DDR4-A17 |
| VCC_PSINTFP_DDR | PS_DDR_A17_504 | | |
| PS_DDR_CS_N0_504 | | AD30 | DDR4-CS |
| PS_DDR_CS_N1_504 | | AD29 | |
| PS_DDR_BA0_504 | | AD27 | DDR4-BA0 |
| PS_DDR_BA1_504 | | AC26 | DDR4-BA1 |
| PS_DDR_BG0_504 | | AC28 | DDR4-BG0 |
| PS_DDR_BG1_504 | | AC27 | DDR4-BG1 |
| PS_DDR_PARITY_504 | | AB26 | DDR4-PAR |
| PS_DDR_RAM_RST_N_504 | | AB25 | DDR4-RESET |
| PS_DDR_ACT_N_504 | | AD26 | DDR4-ACT |
| PS_DDR_ALERT_N_504 | | AB24 | DDR4-ALERT |
| PS_DDR_ZQ_504 | | AB23 | |
| PS_DDR_ODT0_504 | | AB30 | DDR4-ODT0 |
| PS_DDR_ODT1_504 | | AC29 | |

XCZU7EV-1FBVB900E



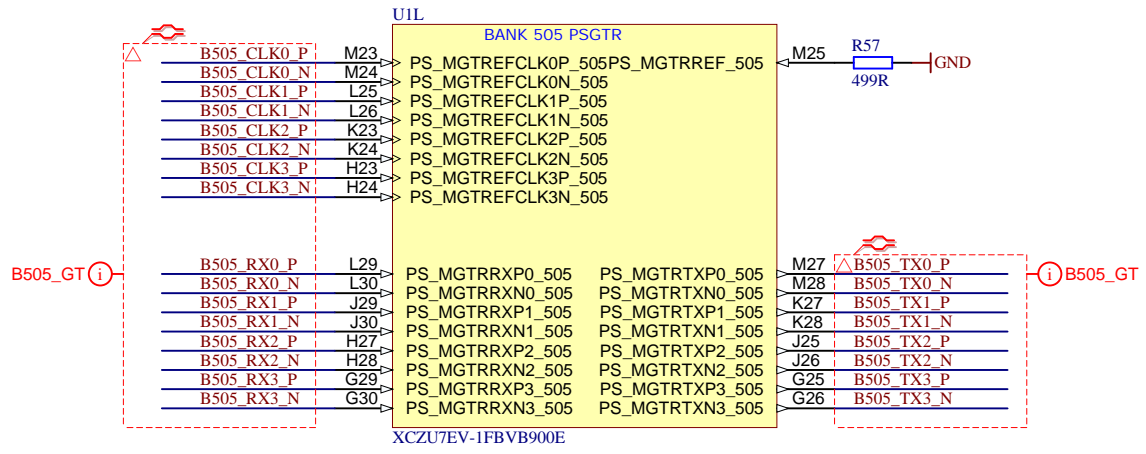
UIK BANK 504 PSDDR

| | | | | | |
|-------------|------|-------------------|-----------------|------|----------|
| DQ0 | AH22 | PS_DDR_DQ0_504 | PS_DDR_DQ32_504 | U24 | DQ32 |
| DQ1 | AH21 | PS_DDR_DQ1_504 | PS_DDR_DQ33_504 | V23 | DQ33 |
| DQ2 | AJ22 | PS_DDR_DQ2_504 | PS_DDR_DQ34_504 | U25 | DQ34 |
| DQ3 | AK22 | PS_DDR_DQ3_504 | PS_DDR_DQ35_504 | V24 | DQ35 |
| DQ4 | AK20 | PS_DDR_DQ4_504 | PS_DDR_DQ36_504 | Y25 | DQ36 |
| DQ5 | AJ19 | PS_DDR_DQ5_504 | PS_DDR_DQ37_504 | AA23 | DQ37 |
| DQ6 | AK19 | PS_DDR_DQ6_504 | PS_DDR_DQ38_504 | AA25 | DQ38 |
| DQ7 | AH19 | PS_DDR_DQ7_504 | PS_DDR_DQ39_504 | Y23 | DQ39 |
| DQ8 | AH23 | PS_DDR_DQ8_504 | PS_DDR_DQ40_504 | P23 | DQ40 |
| DQ9 | AK23 | PS_DDR_DQ9_504 | PS_DDR_DQ41_504 | R23 | DQ41 |
| DQ10 | AG24 | PS_DDR_DQ10_504 | PS_DDR_DQ42_504 | T23 | DQ42 |
| DQ11 | AJ24 | PS_DDR_DQ11_504 | PS_DDR_DQ43_504 | P26 | DQ43 |
| DQ12 | AK26 | PS_DDR_DQ12_504 | PS_DDR_DQ44_504 | T25 | DQ44 |
| DQ13 | AK25 | PS_DDR_DQ13_504 | PS_DDR_DQ45_504 | U23 | DQ45 |
| DQ14 | AG25 | PS_DDR_DQ14_504 | PS_DDR_DQ46_504 | T26 | DQ46 |
| DQ15 | AH26 | PS_DDR_DQ15_504 | PS_DDR_DQ47_504 | P24 | DQ47 |
| DQ16 | AD22 | PS_DDR_DQ16_504 | PS_DDR_DQ48_504 | U26 | DQ48 |
| DQ17 | AE22 | PS_DDR_DQ17_504 | PS_DDR_DQ49_504 | U26 | DQ49 |
| DQ18 | AF22 | PS_DDR_DQ18_504 | PS_DDR_DQ50_504 | U28 | DQ50 |
| DQ19 | AG21 | PS_DDR_DQ19_504 | PS_DDR_DQ51_504 | V27 | DQ51 |
| DQ20 | AD20 | PS_DDR_DQ20_504 | PS_DDR_DQ52_504 | U30 | DQ52 |
| DQ21 | AF20 | PS_DDR_DQ21_504 | PS_DDR_DQ53_504 | V30 | DQ53 |
| DQ22 | AE20 | PS_DDR_DQ22_504 | PS_DDR_DQ54_504 | W30 | DQ54 |
| DQ23 | AG20 | PS_DDR_DQ23_504 | PS_DDR_DQ55_504 | W29 | DQ55 |
| DQ24 | AG23 | PS_DDR_DQ24_504 | PS_DDR_DQ56_504 | R30 | DQ56 |
| DQ25 | AF23 | PS_DDR_DQ25_504 | PS_DDR_DQ57_504 | T30 | DQ57 |
| DQ26 | AF25 | PS_DDR_DQ26_504 | PS_DDR_DQ58_504 | P30 | DQ58 |
| DQ27 | AE23 | PS_DDR_DQ27_504 | PS_DDR_DQ59_504 | P29 | DQ59 |
| DQ28 | AC22 | PS_DDR_DQ28_504 | PS_DDR_DQ60_504 | T28 | DQ60 |
| DQ29 | AC23 | PS_DDR_DQ29_504 | PS_DDR_DQ61_504 | T27 | DQ61 |
| DQ30 | AD25 | PS_DDR_DQ30_504 | PS_DDR_DQ62_504 | P27 | DQ62 |
| DQ31 | AC24 | PS_DDR_DQ31_504 | PS_DDR_DQ63_504 | R27 | DQ63 |
| DDR4-DQS0_P | AJ21 | PS_DDR_DQS_P0_504 | PS_DDR_DQ64_504 | AB29 | |
| DDR4-DQS0_N | AK21 | PS_DDR_DQS_N0_504 | PS_DDR_DQ65_504 | AA30 | |
| DDR4-DQS1_P | AH24 | PS_DDR_DQS_P1_504 | PS_DDR_DQ66_504 | Y30 | |
| DDR4-DQS1_N | AJ24 | PS_DDR_DQS_N1_504 | PS_DDR_DQ67_504 | Y29 | |
| DDR4-DQS2_P | AC21 | PS_DDR_DQS_P2_504 | PS_DDR_DQ68_504 | AA26 | |
| DDR4-DQS2_N | AD21 | PS_DDR_DQS_N2_504 | PS_DDR_DQ69_504 | W27 | |
| DDR4-DQS3_P | AD24 | PS_DDR_DQS_P3_504 | PS_DDR_DQ70_504 | Y27 | |
| DDR4-DQS3_N | AE24 | PS_DDR_DQS_N3_504 | PS_DDR_DQ71_504 | W26 | |
| DDR4-DQS4_P | W24 | PS_DDR_DQS_P4_504 | | | |
| DDR4-DQS4_N | W25 | PS_DDR_DQS_N4_504 | PS_DDR_DM0_504 | AJ20 | DDR4-DM0 |
| DDR4-DQS5_P | P25 | PS_DDR_DQS_P5_504 | PS_DDR_DM1_504 | AJ25 | DDR4-DM1 |
| DDR4-DQS5_N | R25 | PS_DDR_DQS_N5_504 | PS_DDR_DM2_504 | AF21 | DDR4-DM2 |
| DDR4-DQS6_P | U29 | PS_DDR_DQS_P6_504 | PS_DDR_DM3_504 | AE25 | DDR4-DM3 |
| DDR4-DQS6_N | V29 | PS_DDR_DQS_N6_504 | PS_DDR_DM4_504 | Y24 | DDR4-DM4 |
| DDR4-DQS7_P | R28 | PS_DDR_DQS_P7_504 | PS_DDR_DM5_504 | R24 | DDR4-DM5 |
| DDR4-DQS7_N | R29 | PS_DDR_DQS_N7_504 | PS_DDR_DM6_504 | V28 | DDR4-DM6 |
| | Y28 | PS_DDR_DQS_P8_504 | PS_DDR_DM7_504 | P28 | DDR4-DM7 |
| | AA28 | PS_DDR_DQS_N8_504 | PS_DDR_DM8_504 | AA27 | |

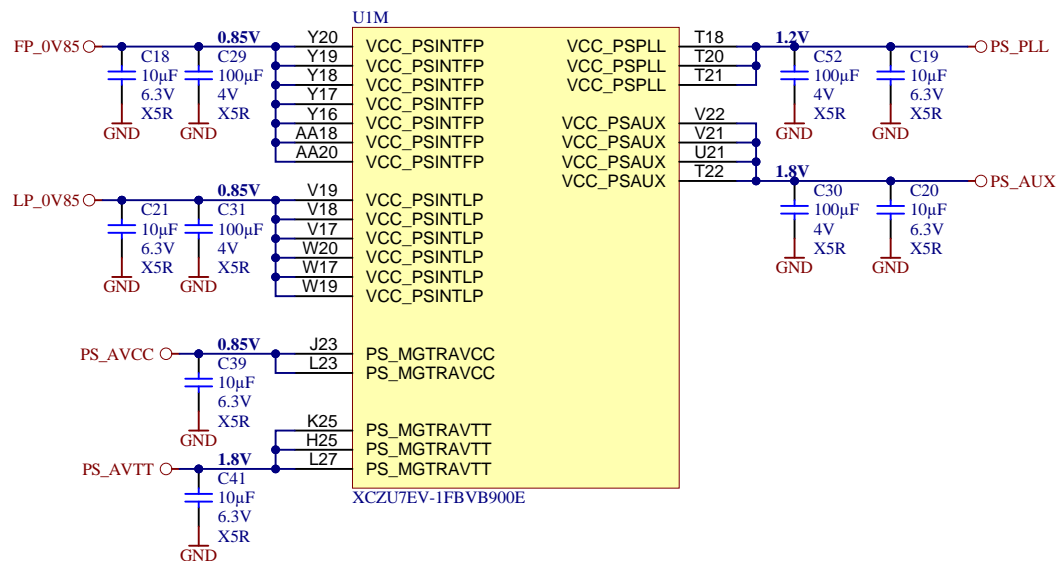
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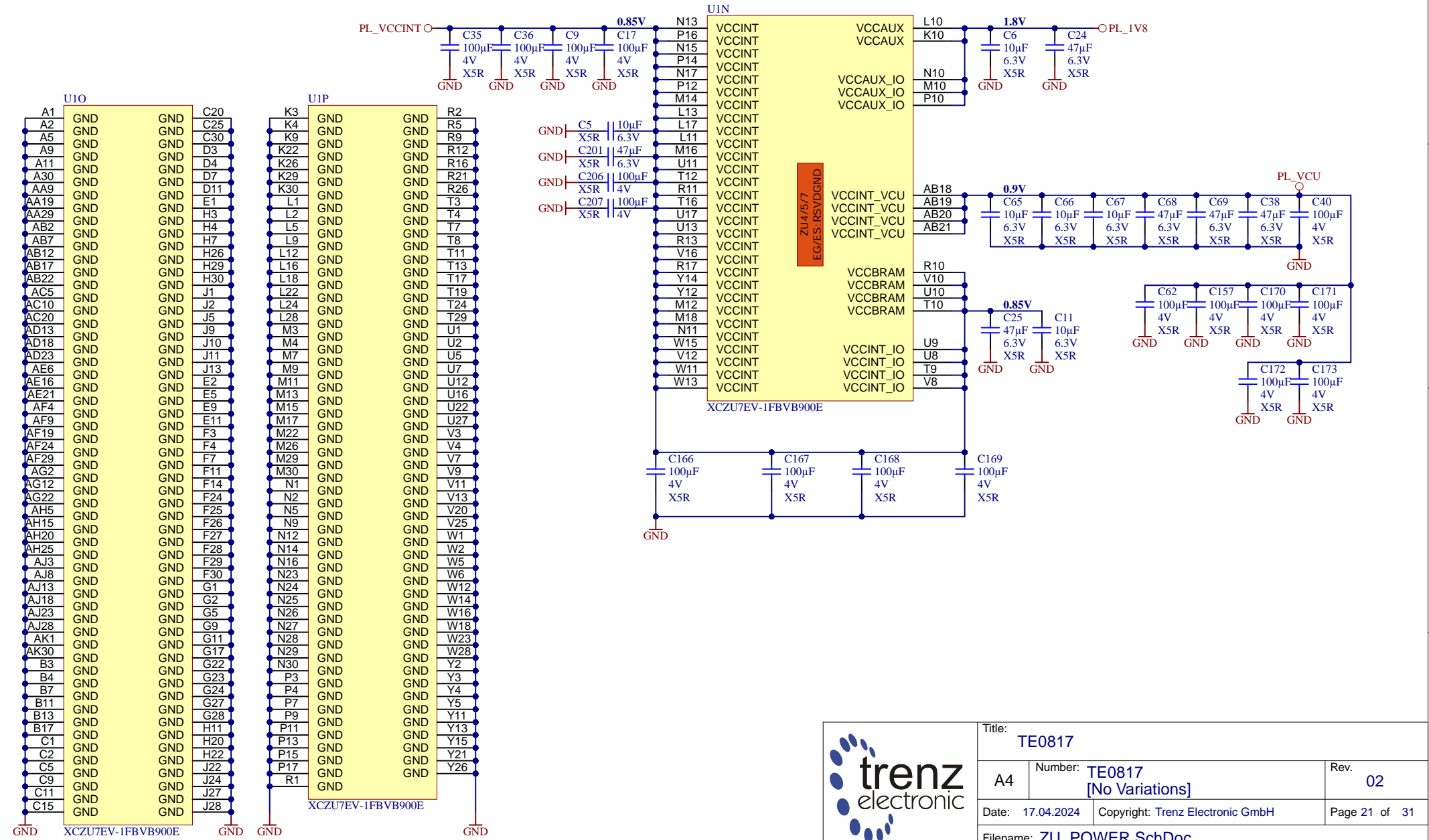
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| Title: TE0817 | | |
| A4 | Number: TE0817 [No Variations] | Rev. 02 |
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| Filename: PS_DDR.SchDoc | | |



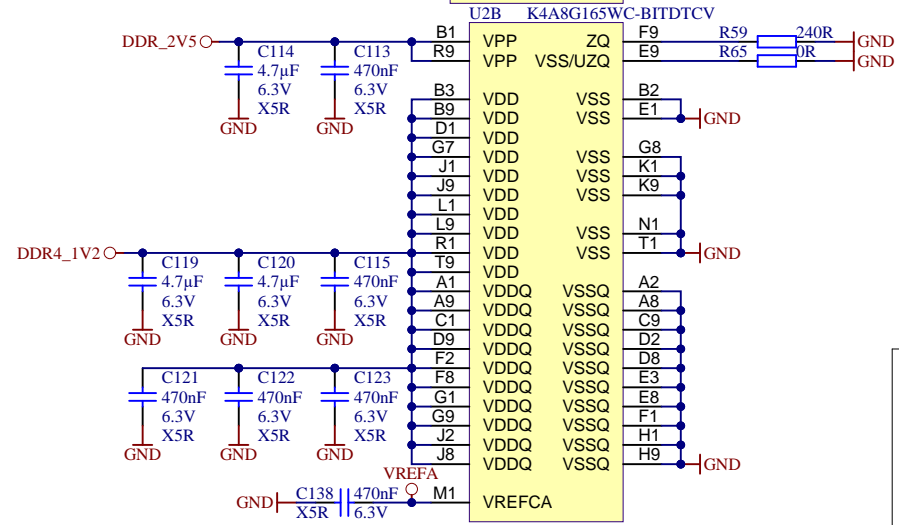
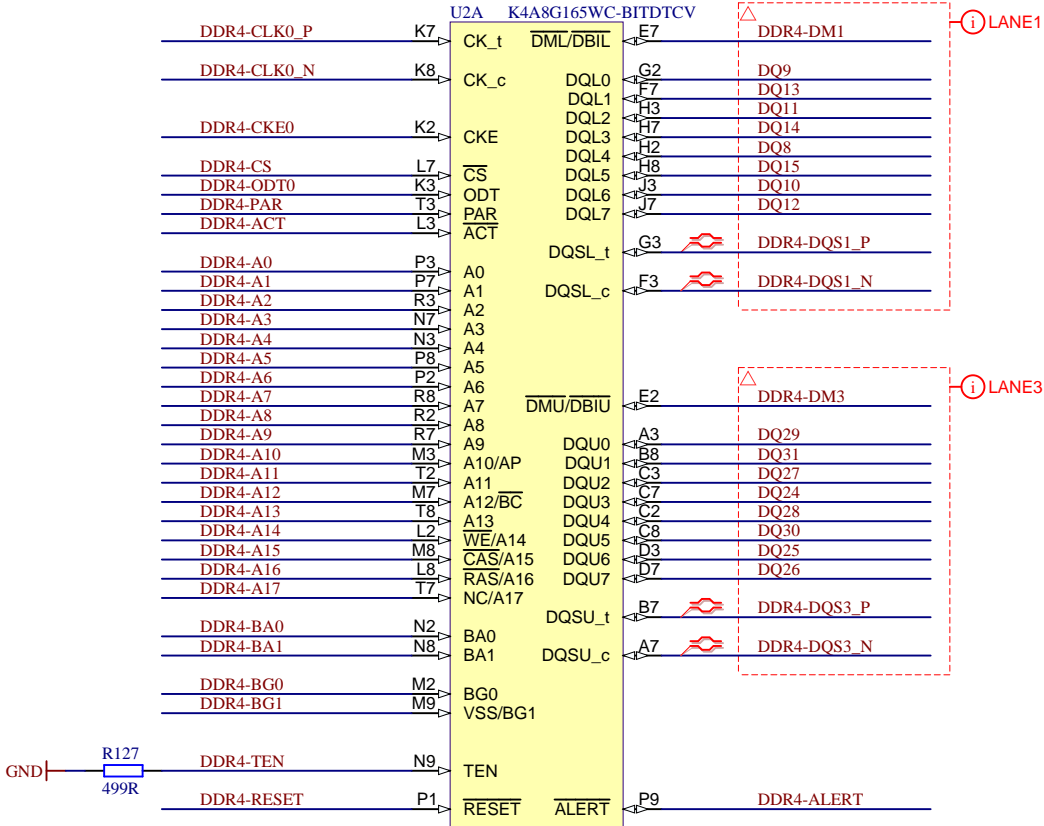
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| | Title: TE0817 | | |
| | A4 | Number: TE0817 [No Variations] | Rev. 02 |
| | Date: 17.04.2024 | Copyright: Trenz Electronic GmbH | Page 19 of 31 |
| | Filename: B_PS_GT.SchDoc | | |



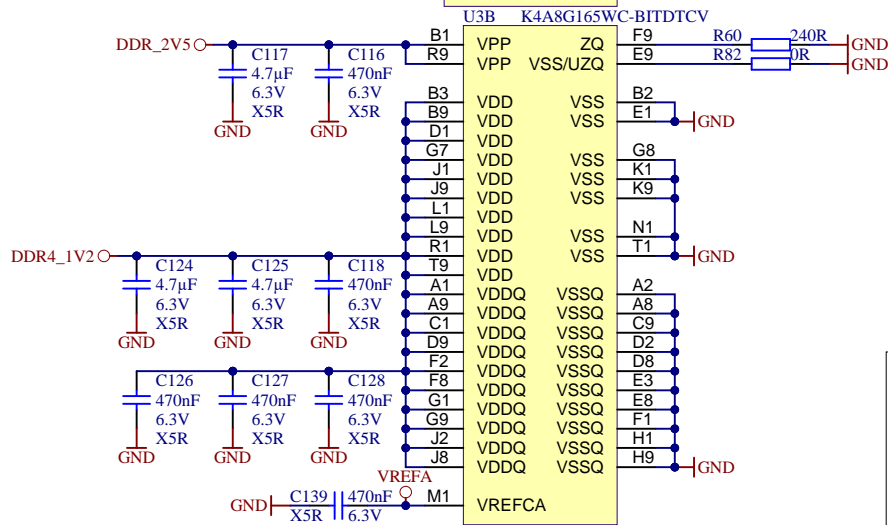
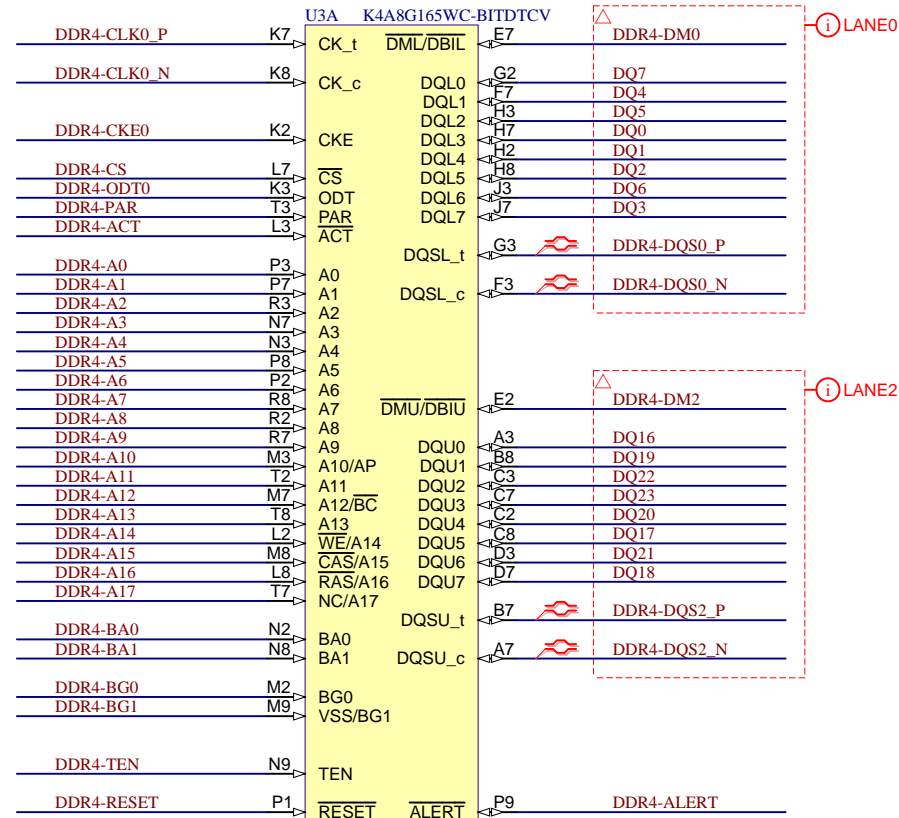
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| A4 | Number: TE0817 [No Variations] | Rev. 02 |
| Date: 17.04.2024 | Copyright: Trenz Electronic GmbH | Page 20 of 31 |
| Filename: ZU_PS_POWER.SchDoc | | |



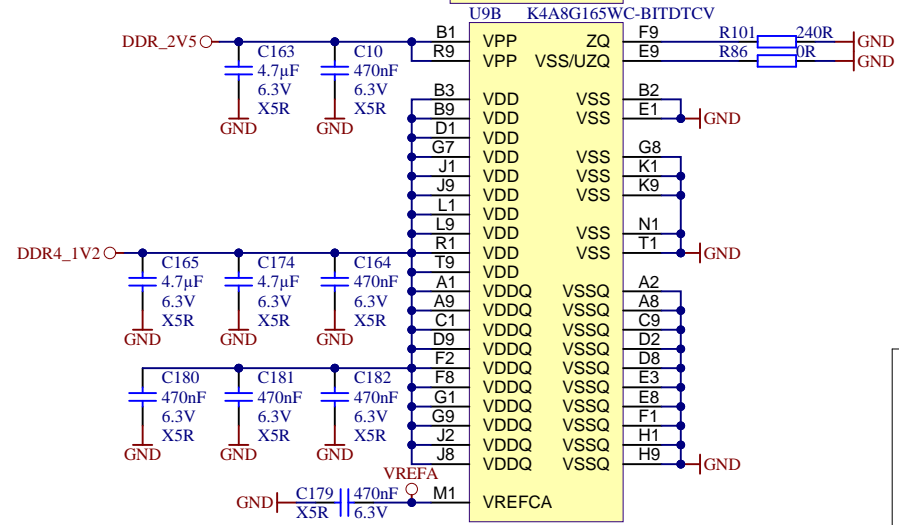
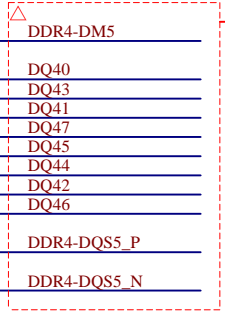
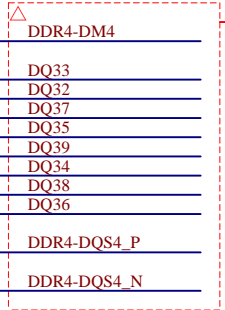
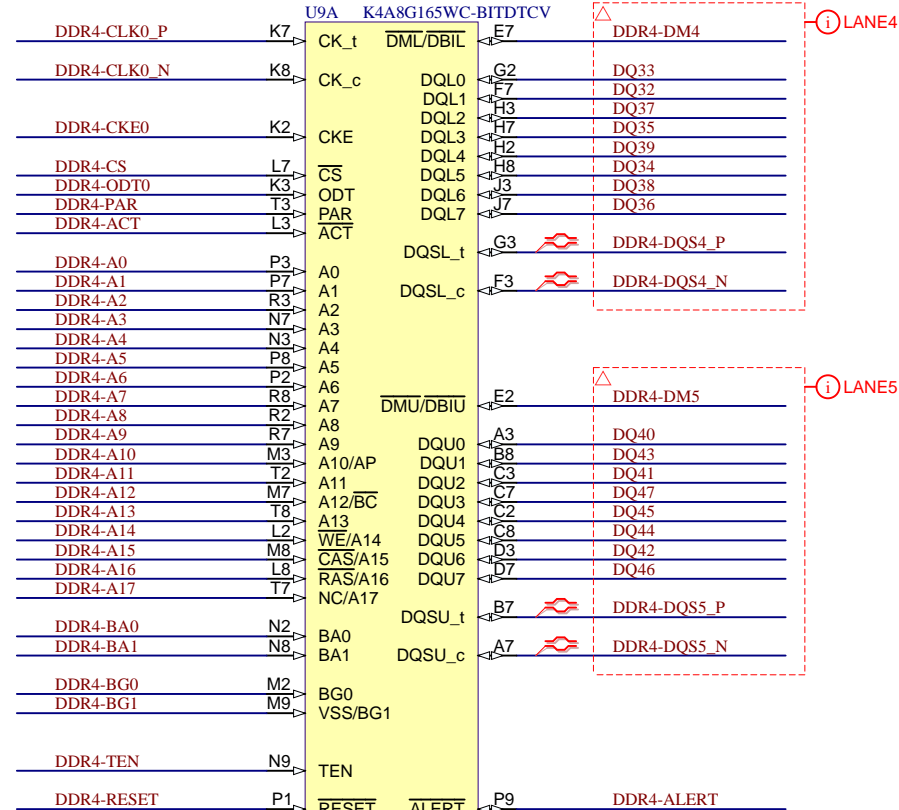
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| Title: TE0817 | | |
| A4 | Number: TE0817 [No Variations] | Rev. 02 |
| Date: 17.04.2024 | Copyright: Trenz Electronic GmbH | Page 21 of 31 |
| Filename: ZU_POWER.SchDoc | | |



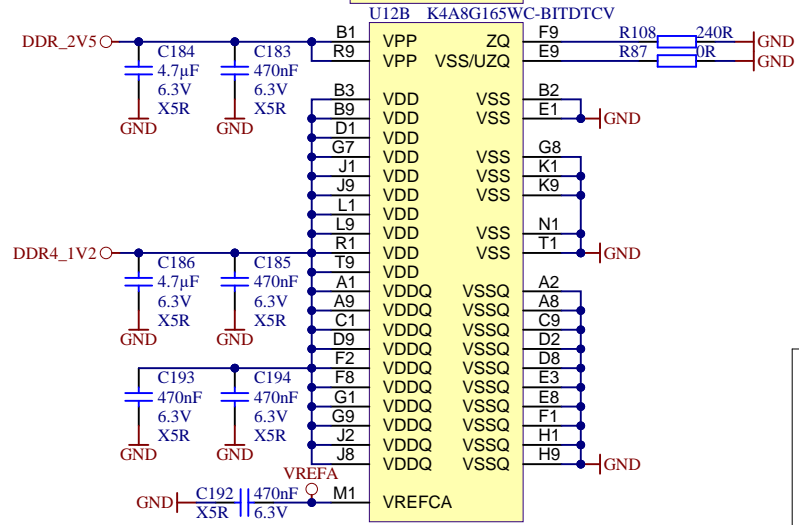
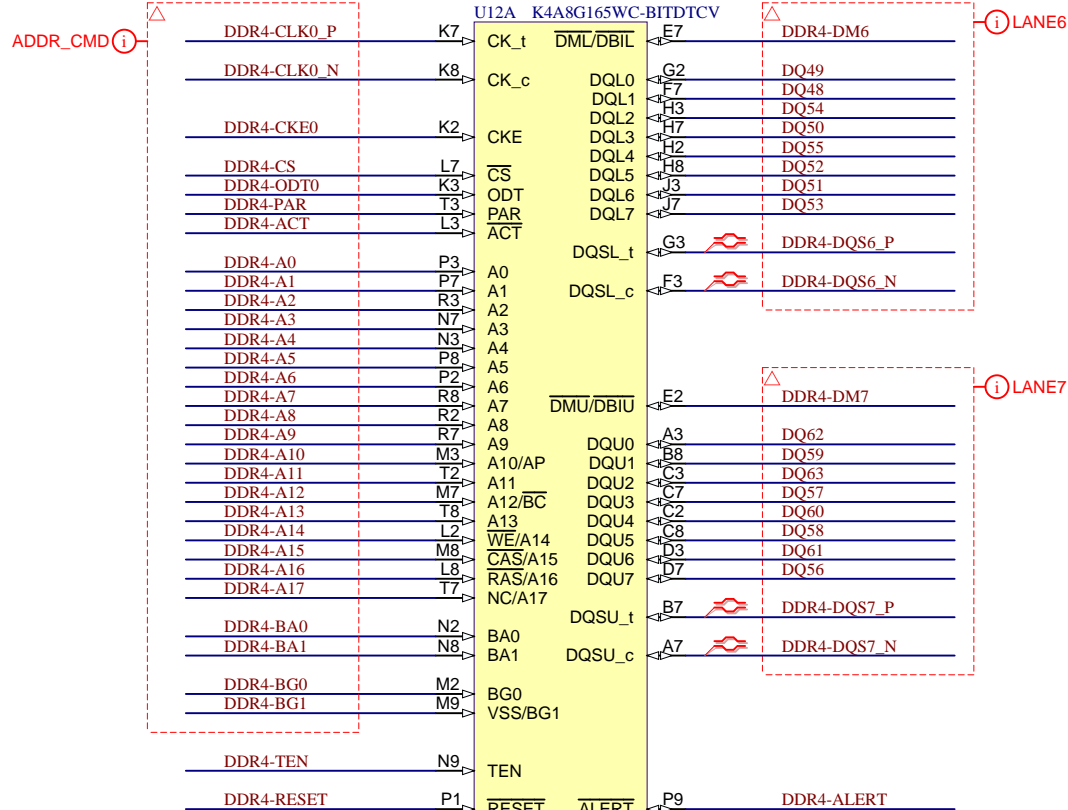
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| A4 | Number: TE0817 [No Variations] | Rev. 02 |
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| Filename: DDR4-RAM.SchDoc | | |



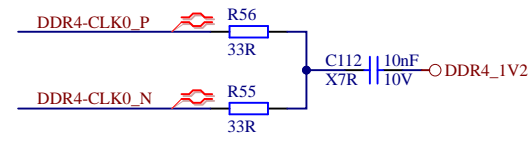
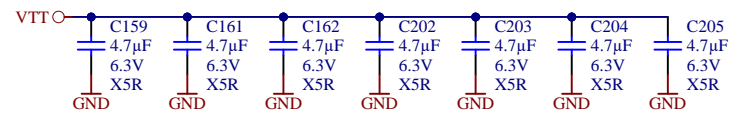
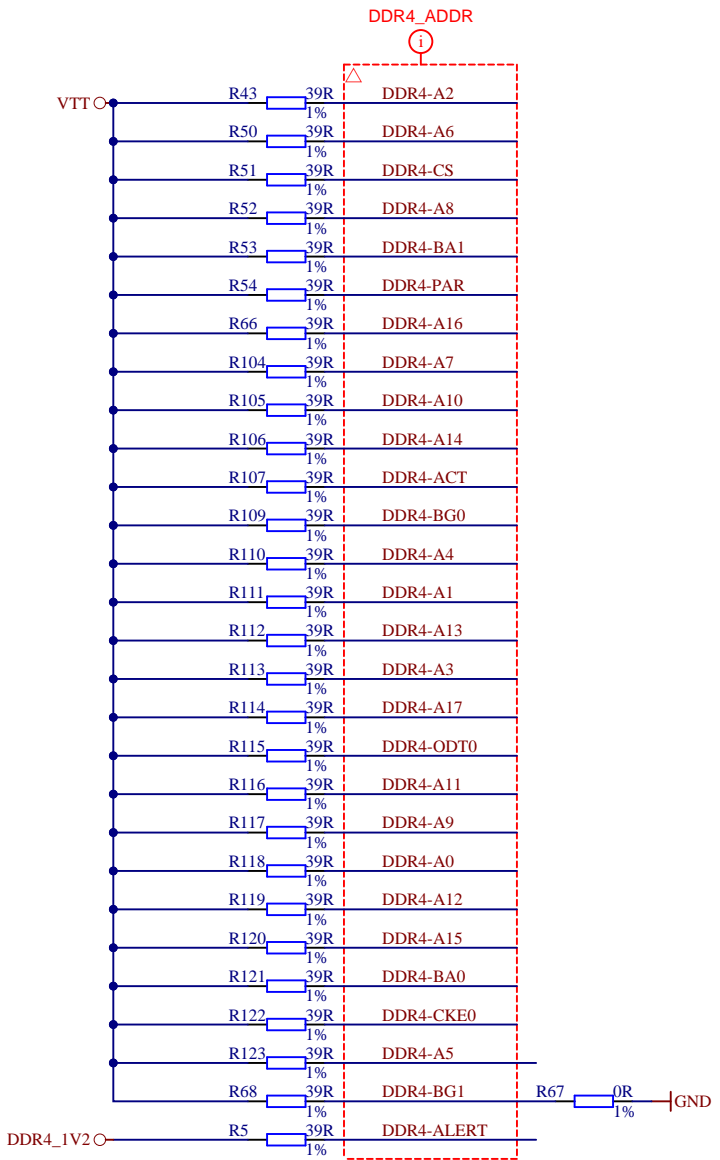
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| A4 | Number: TE0817 [No Variations] | Rev. 02 |
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| Filename: DDR4-RAM_2.SchDoc | | |



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| A4 | Number: TE0817 [No Variations] | Rev. 02 |
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| Filename: DDR4-RAM_3.SchDoc | | |



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| Title: TE0817 | | |
| A4 | Number: TE0817 [No Variations] | Rev. 02 |
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| Filename: DDR4-RAM_4.SchDoc | | |



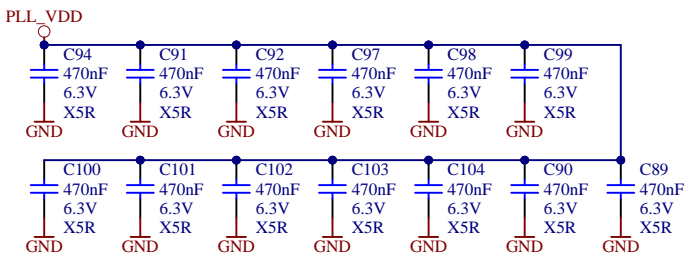
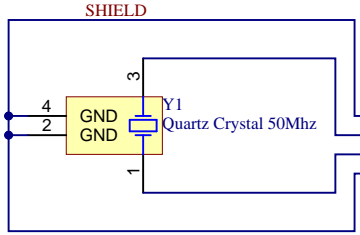
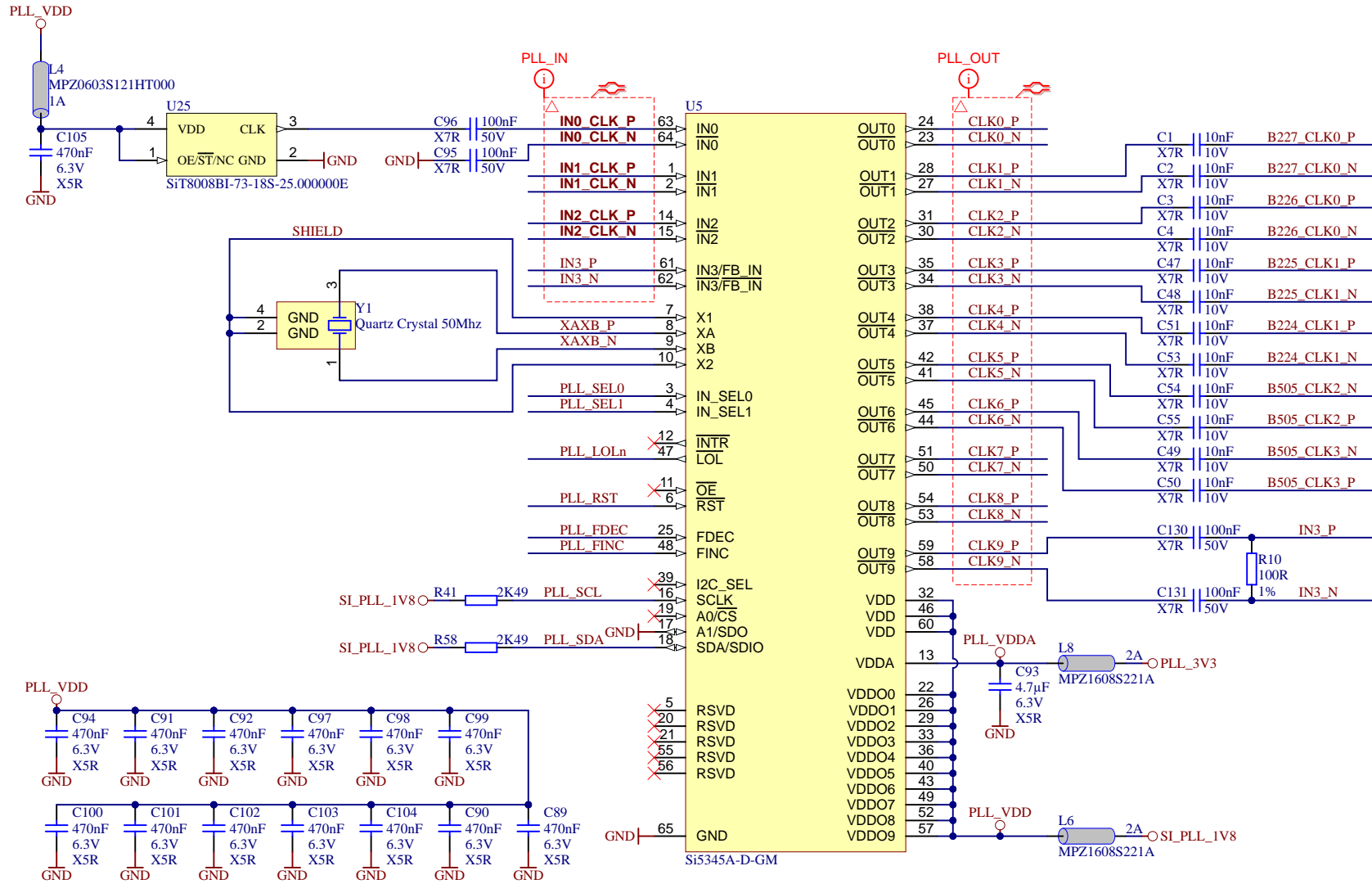
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| Date: 17.04.2024 | Copyright: Trenz Electronic GmbH | Page 26 of 31 |
| Filename: DDR4-TERM.SchDoc | | |

1

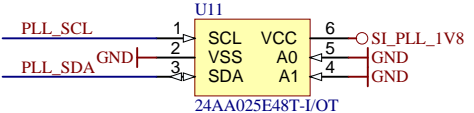
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3

4



EEPROM for MAC



Slave address: 0b1010000



| | | |
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| Title: TE0817 | | |
| A4 | Number: TE0817 [No Variations] | Rev. 02 |
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| Filename: Clock.SchDoc | | |

1

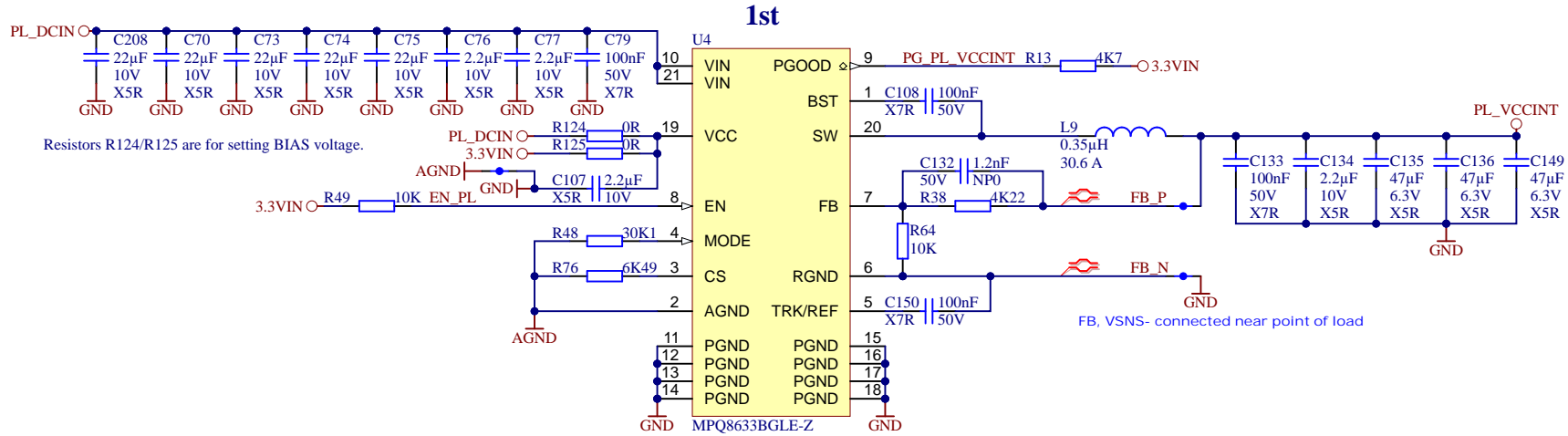
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3

4

U4 can be TPS548A28RWWR or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.

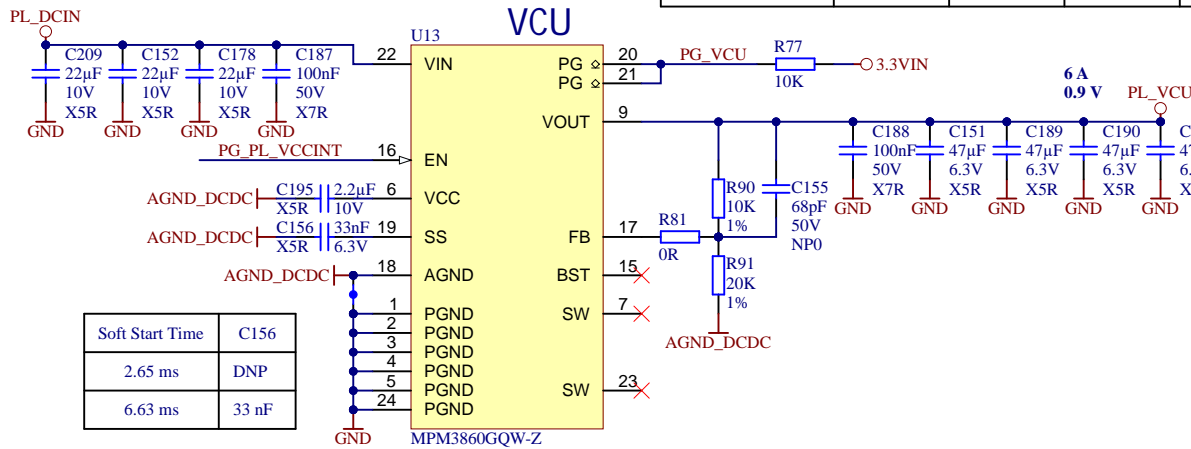
PL VCCINT



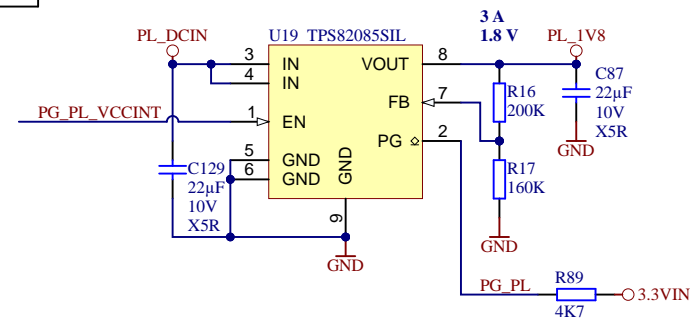
| DCDC U4 (pin compatible) | Current Capability | Current Limit* | R76 | Light-Load Mode | Frequency | R48 | Soft Start Time | C150 |
|--------------------------|--------------------|----------------|-----------|-----------------|-----------|-----------|-----------------|--------|
| TPS548A28 | 15 A | 13.9 A | 4.70 kOhm | CCM | 800 kHz | 30.1 kOhm | 1.66 ms | 100 nF |
| TPS548B28 | 20 A | 19.7 A | 6.49 kOhm | CCM | 800 kHz | 30.1 kOhm | 1.66 ms | 100 nF |
| MPQ8633BGLE-Z | 20 A | 19.7 A | 6.49 kOhm | CCM | 800 kHz | 30.1 kOhm | 1.66 ms | 100 nF |

* Current limit depends on input and output voltage.

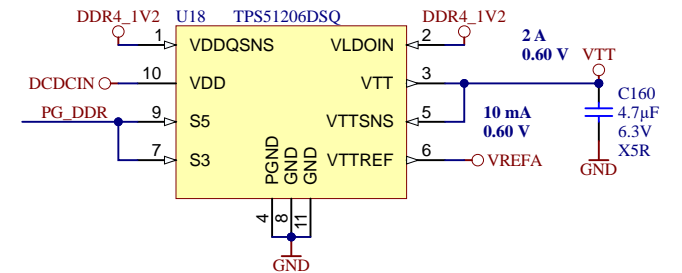
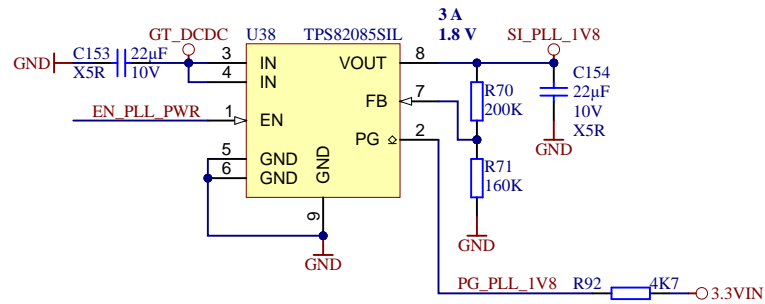
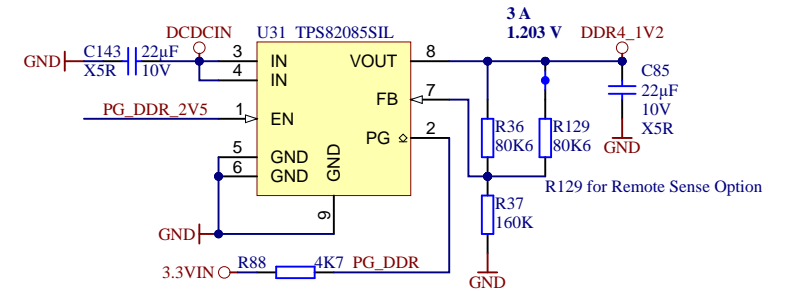
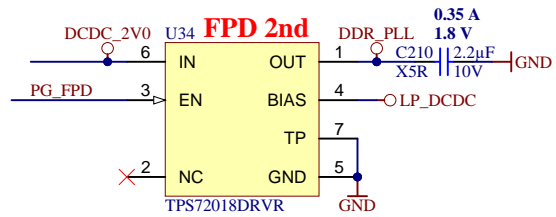
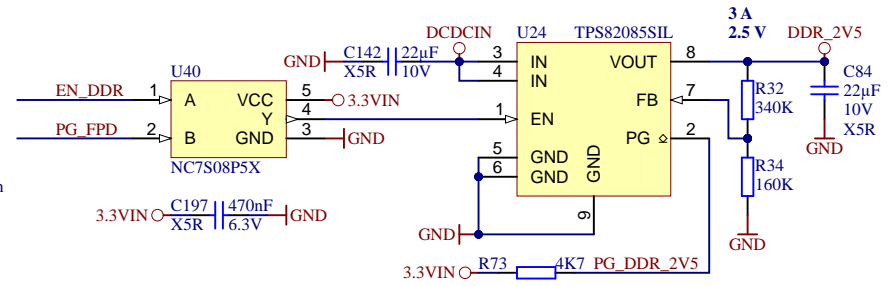
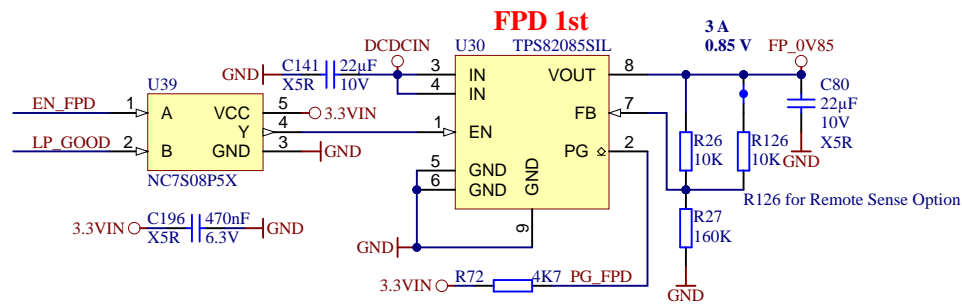
| FPGA Speedgrade | R38 | R64 | PL_VCCINT | C132 |
|-----------------|-----------|---------|-----------|--------|
| -1 | 4.22 kOhm | 10 kOhm | 0.853 V | 1.2 nF |
| -2 | 4.22 kOhm | 10 kOhm | 0.853 V | 1.2 nF |
| -3 | 10 kOhm | 20 kOhm | 0.900 V | 560 pF |



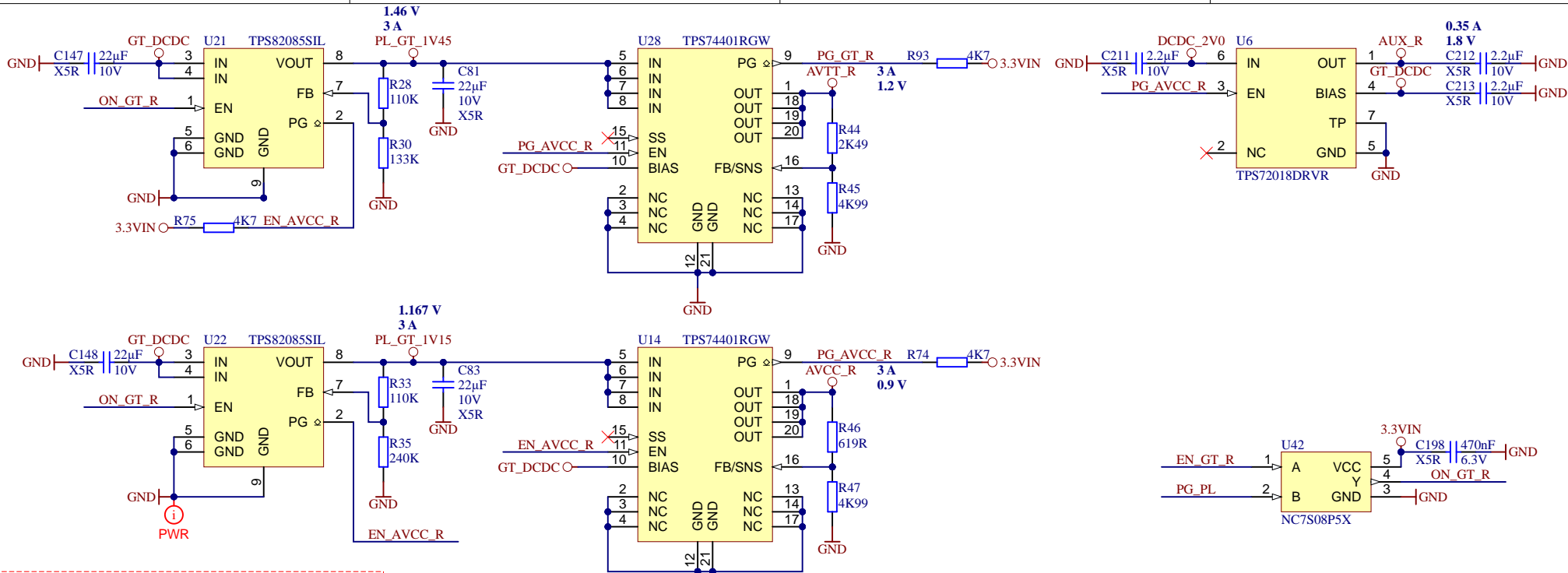
| Soft Start Time | C156 |
|-----------------|-------|
| 2.65 ms | DNP |
| 6.63 ms | 33 nF |



| | | |
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| Title: TE0817 | | |
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Testpoints on top and bottom:

| Testpoints on top: | Testpoints on bottom: |
|--------------------|-----------------------|
| LP_0V85 | TP10 |
| FP_0V85 | TP11 |
| PS_PLL | TP13 |
| PS_GT_1V0 | TP14 |
| PS_AUX | TP21 |
| PS_AVCC | TP22 |
| PS_AVTT | TP33 |
| DDR_PLL | TP34 |
| DDR_2V5 | TP35 |
| VREFA | TP36 |
| VTT | TP4 |
| PL_VCCINT | TP40 |
| DCDC_2V0 | TP42 |
| PL_GT_1V45 | TP44 |
| PL_GT_1V15 | TP47 |
| AUX_R | TP50 |
| AVCC_R | TP52 |
| AVTT_R | TP53 |
| PL_VCU | TP55 |
| 1V8_REFIN | TP57 |
| 1V25_REF | TP60 |
| PLL_VDDA | TP64 |
| PLL_VDD | TP66 |
| SI_PLL_1V8 | TP70 |
| LP_0V85 | TP31 |
| FP_0V85 | TP15 |
| PS_PLL | TP27 |
| PS_GT_1V0 | TP19 |
| PS_AUX | TP29 |
| PS_AVCC | TP30 |
| PS_AVTT | TP28 |
| DDR_PLL | TP18 |
| DDR_2V5 | TP16 |
| VREFA | TP37 |
| VTT | TP23 |
| PL_VCCINT | TP12 |
| DCDC_2V0 | TP17 |
| PL_GT_1V45 | TP45 |
| PL_GT_1V15 | TP48 |
| AUX_R | TP24 |
| AVCC_R | TP26 |
| AVTT_R | TP25 |
| PL_VCU | TP20 |
| 1V8_REFIN | TP58 |
| 1V25_REF | TP61 |
| PLL_VDDA | TP65 |
| PLL_VDD | TP67 |
| SI_PLL_1V8 | TP71 |

Testpoints on top:

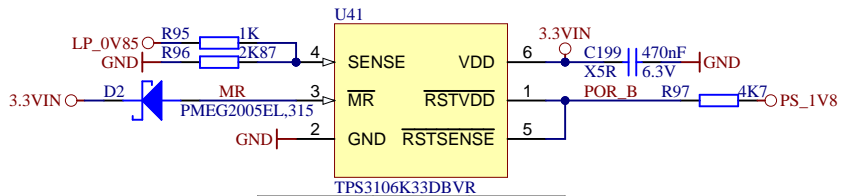
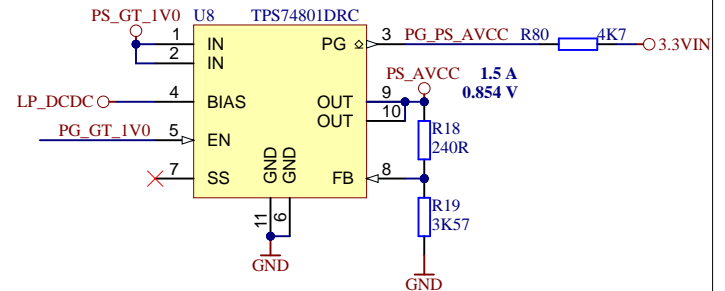
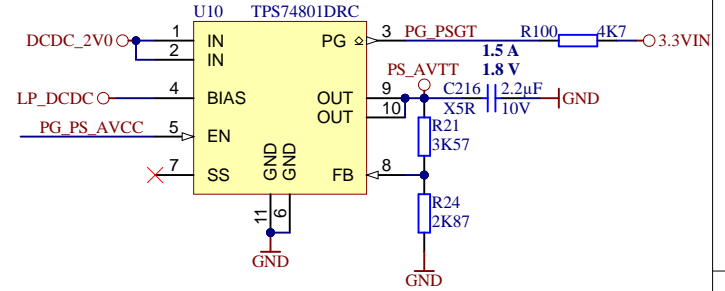
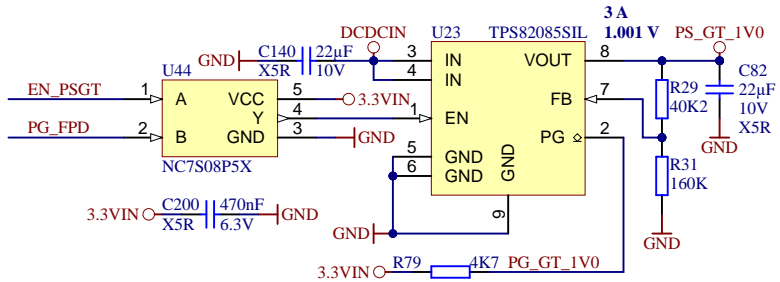
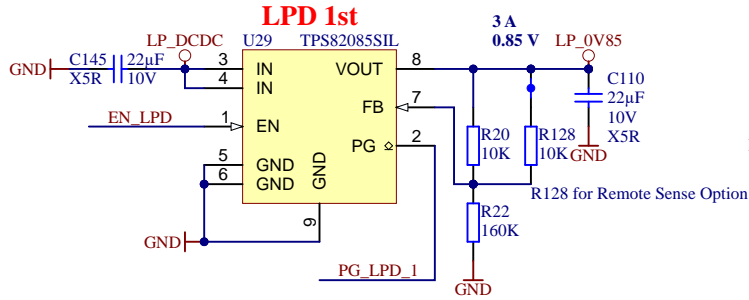
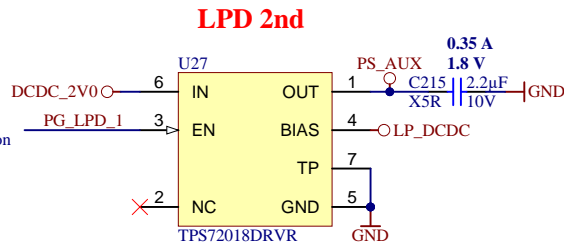
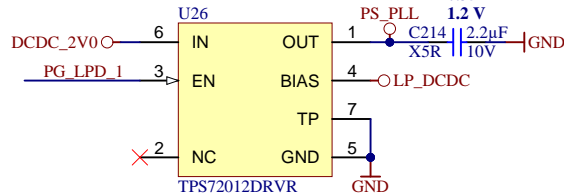
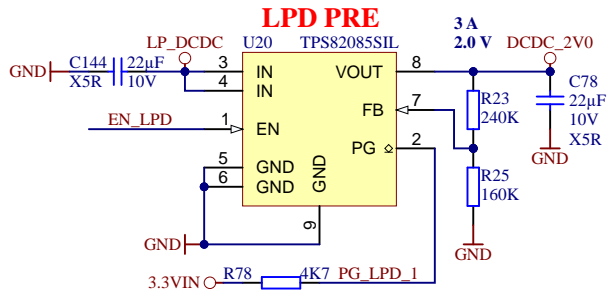
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| 3.3VIN | TP38 |
| LP_DCDC | TP39 |
| DCDCIN | TP41 |
| PL_DCIN | TP43 |
| GT_DCDC | TP46 |
| PLL_3V3 | TP49 |
| PSBATT | TP51 |
| VCCO_47 | TP54 |
| VCCO_48 | TP56 |
| VCCO_64 | TP59 |
| VCCO_65 | TP62 |
| VCCO_66 | TP63 |
| PS_1V8 | TP68 |
| PL_1V8 | TP69 |
| DDR4_1V2 | TP72 |

Testpoints on bottom:

| | |
|----------|------|
| PLL_SCL | TP1 |
| PLL_SDA | TP2 |
| DDR4-TEN | TP3 |
| TCK | TP6 |
| TDI | TP7 |
| TDO | TP8 |
| TMS | TP9 |
| GND | TP5 |
| GND | TP32 |



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| Net Name | Voltage Rail | Low Detect |
|----------|--------------|------------|
| LP_0V85 | 0.85 V | 0.743 V |
| 3.3VIN | 3.3 V | 2.941 V |



| | | |
|---------------------------------|--|----------------|
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| Filename: POWER_4.SchDoc | | |